Improvements of COPPER 500-MHz Flash ADC for PIENU Experiment

Naosuke Ito
Department of Physics, Osaka University

February 4, 2010

Abstract

The measurement of the pion decay branching ratio $R = \Gamma(\pi^+ \to e^+ + \bar{\nu}_e)/\Gamma(\pi^+ \to \mu^+ + \bar{\nu}_\mu)$ is sensitive to the physics beyond the Standard Model of particle physics. The PIENU experiment aims to measure the branching ratio within 0.1% precision, which is better than the precission obtained by the previous experiment by a factor of five or more. It started to take the physics data from April 2009 at the TRIUMF M13 beam line.

The discrimination between two decay modes exceedingly effects the experimental precision. The important information to identify the decay mode is the waveforms of an active target scintillation counter. A COPPER 500-MHz Flash ADC (FADC) system is employed to digitize the waveforms. The subject of my thesis is to improve performance of the FADC system. I achieved to enhance the reliability of the FADC system for synchronizinig channels. Shifts of ADC timing became $< 10^{-9}$ from 10^{-7}-10^{-2} and fluctuations of number of sample points disappeared for $< 10^{7}$ by modifying the firmware. The stability of the reset signal to synchronize all the channels also enhanced. Another part of my thesis consists in updating other COPPER related modules to reflect changes in the trigger system and other DAQ modules readout.

Acknowledgments

I would like to acknoledge Prof. Yoshitaka Kuno for their invaluable advice on physics and experimental technique.

I'm would like to express gratitude to Prf. Masaharu Aoki. I have been a period of excellent learning experiment.

I would also like to thank the valuable contribution made by all the members of Kuno group in Osaka university who helped my research, including, Prof. Akira Sato, Prof. Makoto Yoshida, Prof. Yasushi Arimoto, Prof. Takahisa Itahashi, Prof. Koji Yoshimura, and Wakako Oda.

The members of PIENU group also help me a lot. I appreciate Prof. D. A. Bryman, Prof. T. Numao, Dr. A. Aguilar-Arevalo, Dr. L. Doria, Dr. A. Sher, Dr. D. Vavilov, Prof. Youichi Igarashi, Haotian Pang, Tristan Sullivan, Cameron Hurst, Eric Thwalt.

The members at TRIUMF, Prof. Makoto Fujiwara and Dr. Kentaro Mizouchi made my stay in Canada delightful days.

I'm deeply thankful to Kaoru Yamada and Chloe Malbrunot for everything. I coundn't live another day without their helps and supports for my research and life in Canada .

My thanks go as well to all students, Atsushi Horikoshi, Hideyuki Sakamoto, Taichi Matsumura, Naoyuki Nakadozono, Takuto Tachimoto, Satoshi Takahashi, Eri Matsushita, Takayasu Ebihara, Shunnsuke Hikida, Shinya Araki, Akira Muroi, Noriyuki Miyamoto, Takatomi Yano, Yasutoshi Kuriyama. I enjoyed my school life with them. I would like to express my special appriciation to Naoyuki and Takuto.

Finally, I would like to appreciate my parents. I coundn't finish this thesis without ther supports.

Contents

Acknowledgments **iii**

1 Introduction **1**
1.1 Physics . . . 1
1.1.1 Standard Model Estimation . . . 1
1.1.2 Electron-muon Universality . . . 2
1.1.3 Helicity-unsuppressed Coupling . . . 3
1.1.4 Massive Neutrino . . . 3
1.2 PIENU Experiment . . . 5
1.2.1 Mesurement Method . . . 5
1.2.2 Detector Setup . . . 6
1.2.3 Beam Line . . . 6
1.2.4 Data Acquisition System . . . 7
1.3 Motivation of This Thesis . . . 10
1.3.1 Modification . . . 10
1.3.2 Upgrades . . . 10
1.3.3 Outline of This Thesis . . . 10

2 COPPER 500-MHz Flash ADC System **13**
2.1 COPPER 500-MHz Flash ADC System . . . 13
2.1.1 COPPER 500-MHz Flash ADC Module . . . 13
2.1.2 KEK-VME Crate . . . 19
2.1.3 Clock Distributor Module . . . 19
2.1.4 GPIO Module . . . 21
2.2 Synchronous Signal Setup . . . 23
2.2.1 Setting of Gate Delay in CD . . . 23
2.2.2 Setting of Reset Delay in CD . . . 23
2.2.3 Logic for Synchronizing Test . . . 25

3 Modifications of FINESSE 500 MHz FADC **27**
3.1 Issues of FINESSE 500 MHz FADC . . . 27
3.2 Shift of ADC timing . . . 27
3.2.1 Issue . . . 27
3.2.2 Modification . . . 36
3.2.3 Results . . . 40
3.3 Fluctuation of Number of Sample Points . . . 41

3.3.1 Issue . . . 41
3.3.2 Modification . . . 46
3.3.3 Result . . . 46
3.4 Small Margin of Reset Timing . . . 48
3.4.1 Issue . . . 48
3.4.2 Mdification . . . 48
3.4.3 Results . . . 51
3.5 Summary . . . 55

4 Upgrades of COPPER 500-MHz FADC System **57**
4.1 Motivations of COPPER 500-MHz FADC System Upgrade . . . 57
4.2 Level 0+1 Trigger by GPIO Firmware Upgrade . . . 57
4.2.1 Digital Sum Trigger Module Installation . . . 57
4.2.2 Level 0+1 Trigger by GPIO Firmware Update . . . 58
4.2.3 Tests of Level 0+1 Trigger . . . 65
4.3 Time Stamp FINESSE 500-MHz FADC Firmware Upgrade . . . 68
4.3.1 Read-out System Update . . . 68
4.3.2 Time Stamp by FINESSE Firmware Update . . . 69
4.3.3 Tests of Time Stamp . . . 69
4.4 Summary . . . 72

5 Summary **73**

List of Figures

1.1 Diagram of the pion decay . . . 2
1.2 Bounds on $\mid V_{e4} \mid^2$ versus m_4. . . . 4
1.3 Schematics of the PIENU detector . . . 5
1.4 PIENU detector . . . 6
1.5 Schematics of M13 beam line . . . 7
1.6 M13 beam line . . . 7
1.7 PIENU trigger diagram . . . 8
1.8 Typical wave form in the target . . . 9
1.9 Positron timing distributions from pion decays . . . 10

2.1 The layout of the COPPER mother board. . . . 15
2.2 FINESSE 500-MHz FADC . . . 16
2.3 Schematic diagram of the data flow in FINESSE 500-MHz FADC . . . 18
2.4 KEK-VME with the COPPER board . . . 19
2.5 Schematic diagram of Clock Distributor . . . 20
2.6 Clock Distributor . . . 22
2.7 GPIO . . . 22
2.8 Diagram of connections between CD and COPPER to synchronize . . . 23
2.9 Diagram to determine the write enable (WEN) region by a gate signal (GATE) . . . 24
2.10 Diagram to determine the phase of 125 MHz write clock (WCLK) from ADCs to FIFOs by reset (RST) . . . 24
2.11 Logic diagram to make the synchronous signals . . . 25
2.12 The waveforms of the synchronous signals . . . 26

3.1 Waveform with time offset shift between two ADCs . . . 28
3.2 Schematics of one channel data from two ADCs and two FIFOs . . . 28
3.3 Diagram to read and write the data from FINESSE FIFOs to COPPER FIFOs . . . 29
3.4 Scheme to create the endcode . . . 30
3.5 Endcode Error versus temperature in the electronics rack . . . 30
3.6 The difference between the triggers with and without the endcode error . . . 32
3.7 Positron energy spectra in NaI with and without endcode errors . . . 32
3.8 Schematics of two channel data from four ADCs and four FIFOs . . . 34
3.9 Timing chart to write one channel data on two FIFOs . . . 35
3.10 Diagram of signal lines and modules for clocks of Xilinx FPGA . . . 37
3.11 Quadrant Phase Shift Outputs Shift CLKIN, Each by a Quarter Period . . . 38
3.12 BUFGMUX . . . 39

3.13 Update of switching the read clock (RCLK) to the FIFO from 42 MHz to 125 MHz . . 40
3.14 Number of sample versus event ID for four FINESSEs 42
3.15 Diagram to send and dump the data 43
3.16 Logic diagram to buffer the data 44
3.17 The number of sample at various gate delay settings through the previous firmware . . 44
3.18 The timings of synchronous signal edges for four COPPERs at various reset delay settings through the previous firmware 44
3.19 Timing chart of the gate (GATE), write enable (WEN), and read enable (REN) signals latched by the same clock timing 45
3.20 Diagram of a latched gate signal (latched GATE) distribution in FPGA 46
3.21 Timing chart of shorter gate (GATE), write enable (WEN), and read enable (REN) with latched GATEs 47
3.22 Diagram to reset the ADCs & Clocks 48
3.23 Schematics and diagram of the reset lines with different length 49
3.24 The timings of synchronous signal edges at various reset delay settings through the previous and modified firmware 50
3.25 Diagram of selecting gate or reset from FINESSE input 51
3.26 Reset enable signal 52
3.27 Timing chart of the reset from gate input AND the reset enable from the trigger card . 53
3.28 The timings of synchronous signal edges for four COPPERs at various reset delay settings through a modified firmware 54

4.1 Schematic diagram of the trigger delay by TIGC 58
4.2 PIENU trigger diagram upgrade 60
4.3 Logic diagram upgrade for COPPER in PIENU 62
4.4 Level 1 trigger 63
4.5 Level 0 + 1 trigger 64
4.6 Auto clear 66
4.7 Left: Waveform of the NaI calorimeter with LV1 trigger. Righ: Waveform of the NaI calorimeterwith LV 0 + LV 1 trigger 67
4.8 Schematics of DAQ network 68
4.9 Timing chart of the time stamp 70
4.10 Time stamp versus event number 70
4.11 Difference of timestamps between an event and the next event 71
4.12 Difference of timestamps between four FINESSEs. 71
4.13 Event ID versus Timestamp 71

List of Tables

1.1 A summary of e-μ universality test 2

2.1 Specificaitons of the COPPER mother board 14
2.2 Specifications of FINESSE 500-MHz FADC card. 17
2.3 IC chips used in the FINESSE 500-MHz FADC card. 17
2.4 Specifications of the Clock Distributor 20
2.5 GPIO features 21

3.1 Bias test by trigger 31
3.2 Bias test by NaI analysis 31
3.3 BUFGMUX 36

4.1 VME readout time & live time 69

Chapter 1

Introduction

1.1 Physics

The branching ratio between $\pi^+ \to e^+ + \bar{\nu}_e$ and $\pi^+ \to \mu^+ + \bar{\nu}_\mu$ ($R = \Gamma(\pi^+ \to e^+ + \bar{\nu}_e)/\Gamma(\pi^+ \to \mu^+ + \bar{\nu}_\mu)$) provides the best test of the hypothesis of electron-muon universality in weak interactions and is sensitive to new interactions with the mass scales up to 1000 TeV. Any differences between the calculated and the experimentally obtained branching ratio are proofs of the lepton universality violation or new helicity unsuppressed interactions. The pion decay is also sensitive to massive neutrinos because the energy of positron from $\pi \to e$ decay with the massive neutrino is lower than the $\pi^+ \to e^+ + \bar{\nu}_e$ decay.

The observable branching ratio R is very precisely calculated by Standard Model (SM) as

$$R_{e/\mu}^{SM} = 1.2353(1) \times 10^{-4}. \tag{1.1}$$

On the other hand, the experimental values are

$$R_{e/\mu}^{TRIUMF} = (1.2265 \pm 0.0034(stat) \pm 0.0044(syst)) \times 10^{-4}, \tag{1.2}$$

$$R_{e/\mu}^{PSI} = (1.2346 \pm 0.0035(stat) \pm 0.0036(syst)) \times 10^{-4}, \tag{1.3}$$

from experiments performed at TRIUMF and PSI, respectively. The errors of these experimental values are almost fifty times larger than that of calculation. The purpose of the PIENU experiment is to improve the precision of the measurement by a factor of more than five to give less than 0.1% of accuracy.

1.1.1 Standard Model Estimation

$R_{e/\mu^{SM}}$ is one of the most precisely calculated value in the Standard Model. In lowest order, the $\pi^+ \to e^+ + \bar{\nu}_e$ branching ratio $R_{e/\mu}^0$ is calculated to be

$$R_{e/\mu}^0 = \frac{m_e^2}{m_\mu^2}\left(\frac{m_\pi^2 - m_e^2}{m_\pi^2 - m_\mu^2}\right)^2 = 1.28347 \times 10^{-4}. \tag{1.4}$$

The smallness of $R_{e/\mu}$ is a consequence of the helicity suppression coming from the V-A current structure of the weak interaction and the absence of the right-handed neutrinos Since the observed branching ratio includes the effect of physical and virtual photons, knowledge of radiative corrections to

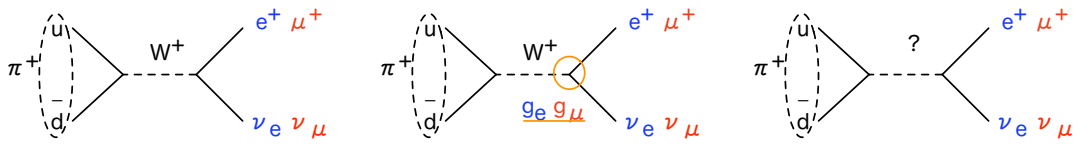

Figure 1.1: Diagram of the pion decay. left: Diagram of the pion decay through the Standard Model. middel: Diagram of the pion decay with the Non-Universality. right: Pion Decay through the Helicity-unsuppressed Coupling.

the branching ratio is important in order to extract the ratio of the coupling constants. Early calculations for the radiative process assuming a point-like pion showed that the correction was the order of $\sigma = (3\alpha/\pi)\ln(m_e/m_\mu)$, which reduced the calculated branching ratio to $R^{th}_{e/\mu} = 1.233 \times 10^{-4}$. The major uncertainties of the calculations are in the divergences and pion-structure dependence. After including small structure dependent effects and the leading 2-loop logarithmic corrections one finds the SM prediction as shown in Equation (1.1) The error is very small but still quite conservative.

1.1.2 Electron-muon Universality

Electron-muon universality, within the context of the SM, refers to the fact that those charged leptons have identical electroweak gauge interactions. It means the coupling constants g_e and g_μ in Figure 1.1 (middle) are exactly the same. If the $e-\mu$ universality does not hold, $R^0_{e/\mu}$ can be expressed as

$$R^0_{e/\mu} = \frac{g_e^2}{g_\mu^2}\frac{m_e^2}{m_\mu^2}\left(\frac{m_\pi^2 - m_e^2}{m_\pi^2 - m_\mu^2}\right)^2, \tag{1.5}$$

which is different from Equation (1.1) by factor g_e^2/g_μ^2. Therefore, the $e-\mu$ universality can be studied by comparing the experimentally obtained R and theoretical R. The $e-\mu$ universality in the charged current mode has been studied with π, τ and W leptonic decays as summarized in Table 1.1. The most stringent test of $e-\mu$ universality comes from the measurements of the branching ratio between $\pi^+ \to e^+ + \bar{\nu}_e$ and $\pi^+ \to \mu^+ + \bar{\nu}_\mu$ followed closely by the measurement of τ decay. Marciano[7] has pointed out that the branching ratios, $\Gamma(\pi \to e\nu)/\Gamma(\pi \to \mu\nu)$ and $\Gamma(K \to e\nu)/\Gamma(K \to \mu\nu)$, are sensitive to the longitudinal component of the W coupling (scalar and vector), while the others test the transverse component (vector).

Table 1.1: A summary of e-μ universality test.

Process	g_e/g_μ		
π decay	0.9985	$\pm$	0.0016
K decay	0.994	$\pm$	0.022
τ decay	0.9999	$\pm$	0.0021
ν_e, ν_μ scattering	1.10	$\pm$	0.05
W decay	0.999	$\pm$	0.011

1.1.3 Helicity-unsuppressed Coupling

The PIENU experiment is extremely sensitive to helicity-unsuppressed couplings such as the pseudo-scalar coupling in Figure 1.1 (right) because the Standard Model asumes only helicity-suppression in the $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay. Since the pseudo-scalar contribution comes as an interference term with the dominant axial-vector term, the contribution is proportional to $1/m_H^2$, where m_H is the mass of a hypothetical particle while this is in contrast to $1/m_H^4$ dependence in lepton flavour violating decays. The deviation of the new branching ratio from the SM prediction can be parameterized as

$$1 - \frac{R_{e/\nu}^{Exp}}{R_{e/\nu}^{SM}} \sim \pm \frac{\sqrt{2}\pi}{G_\mu} \frac{1}{\Lambda_{eP}^2} \frac{m_\pi^2}{m_e(m_d + m_u)} \sim \left(\frac{1TeV}{\Lambda_e P}\right)^2 \times 10^3 \tag{1.6}$$

but ignoring small contributions from $\pi^+ \rightarrow \mu^+ + \bar{\nu}_\mu$ decay and a presence of pseudoscalar interactions are needed. Λ_{eP} is a mass scale of new pseudoscalar interaction in $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay. This makes the measurement of a 0.1% level of the pion branching ratio sensitive to the mass scales up to 1000 TeV for pseudo-scalar interaction through loop corrections.

1.1.4 Massive Neutrino

The PIENU experiment can also contribute to search for massive neutrinos in the mass region 50 to 130 MeV/c^2 by the positron spectrum from $\pi \rightarrow e$ decay. Neutrinos are revealed to have mass by the K2K experiment but the smallness is not still understood. The search for massive neutrino will clarify the neutrino physics.

The positron energy from $\pi \rightarrow e$ decay can reconstruct the massive neutrino mass by

$$m_\nu = \sqrt{m_\pi^2 + m_e^2 - 2m_\pi E_e}. \tag{1.7}$$

The peak search for other than 69.8 MeV can directly prove the massive neutrino mass because of the two bady decays. Figure 1.2 shows the current limit of the mixing parameter[2]. The parameter is defined by

$$\nu_l = \sum_{i=1}^{3+k} V_{li}\nu_i \quad (l = e, \mu, \tau). \tag{1.8}$$

The previous experiment to study the pion decay is next to the neutrinoless double beta decay around 100 MeV/c^2. The double beta decay experiment, however, needs Majorana neutrinos while the pion decay is detectable to other type of neutrions. Improved statistics and rejections of background in PIENU will set a stronger limit on the existence of massive neutrinos in the mass region.

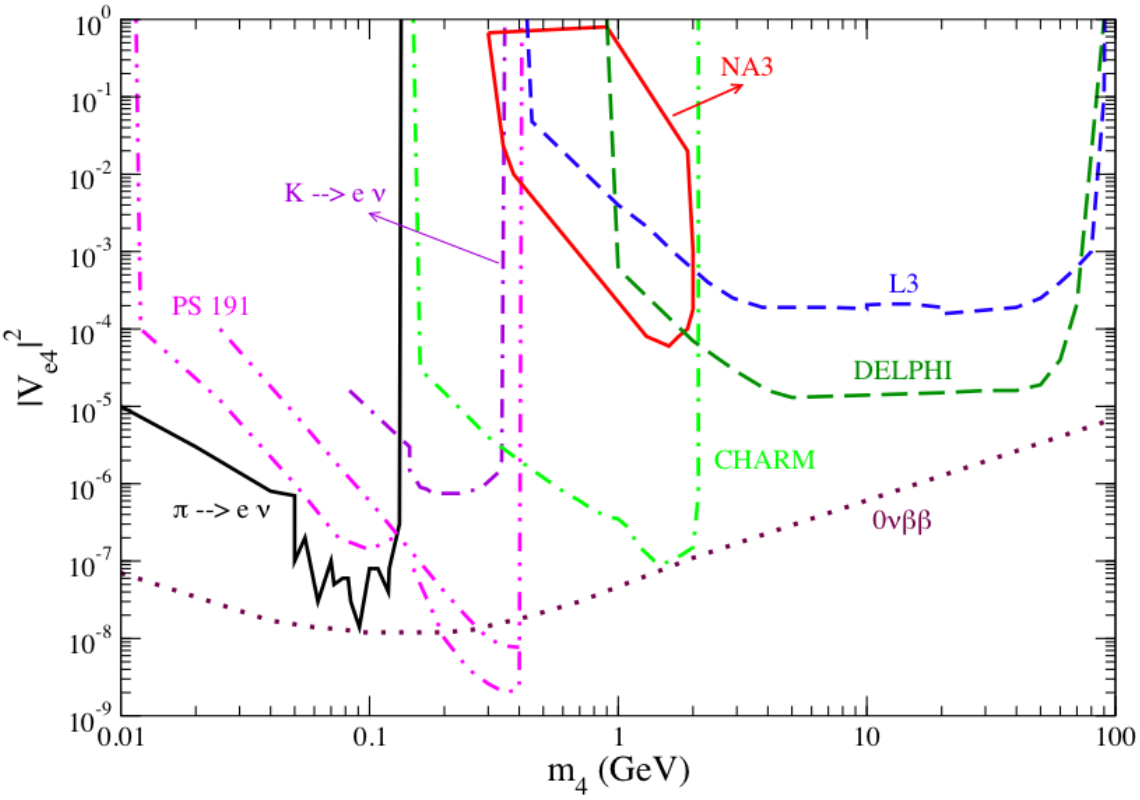

Figure 1.2: Bounds on $\mid V_{e4} \mid^2$ versus m_4.

1.2 PIENU Experiment

The PIENU experiment is aiming to measure the branching ratio between $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ and $\pi^+ \rightarrow \mu^+ + \bar{\nu}_\mu$ decays by 0.1% precision. It employs the improved experimental technique, which is used by the previous experiment at TRIUMF in the early 90's. Improvements lie detectors, Data Acquisition (DAQ) system, and simulations. A new calorimeter and a beam extension made it possible to increase the statistics with 20% solid angle for the large acceptanse and the clean pion beam. Tracking and waveform digitiging also had been studied to reduce the systematic errors by the detailed identification of particles. This section shows the methods and equipments.

1.2.1 Mesurement Method

Fitting of decay time spectra of positrons from $\pi \rightarrow e$ and $\pi \rightarrow \mu \rightarrow e$ decays provides the branching ratio. The decays are identified by a positron energy, waveforms in the target scintillators, and trackings of both incoming and out going particles.

The positron energy from the $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ and $\pi^+ \rightarrow \mu^+ + \bar{\nu}_\mu$ decays are respectively $T_{e^+} = 69.3$ MeV ($\pi \rightarrow e$) and $T_{e^+} = 0 - 52.3$ MeV ($\pi \rightarrow \mu \rightarrow e$) because of the difference between the two bady decay from $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ and the Mitchell spectrum of the muons from $\pi \rightarrow \mu \rightarrow e$. The pulse fitting of the waveforms in target scintillators can also distinguish the two decays and backgrounds by the different numbers of particle hits. The vertices between incident pion and decay positron also identify the decays. It is detected by the upstream and downstream position detectors, the wire chambers (WCs) and the silicon-strip (Si) detectors. Furthermore, the vertex method also contributes to suppress the events whose pion decays in the flight. The events is one of major background. The Si detectors will to sufficiently decrease them.

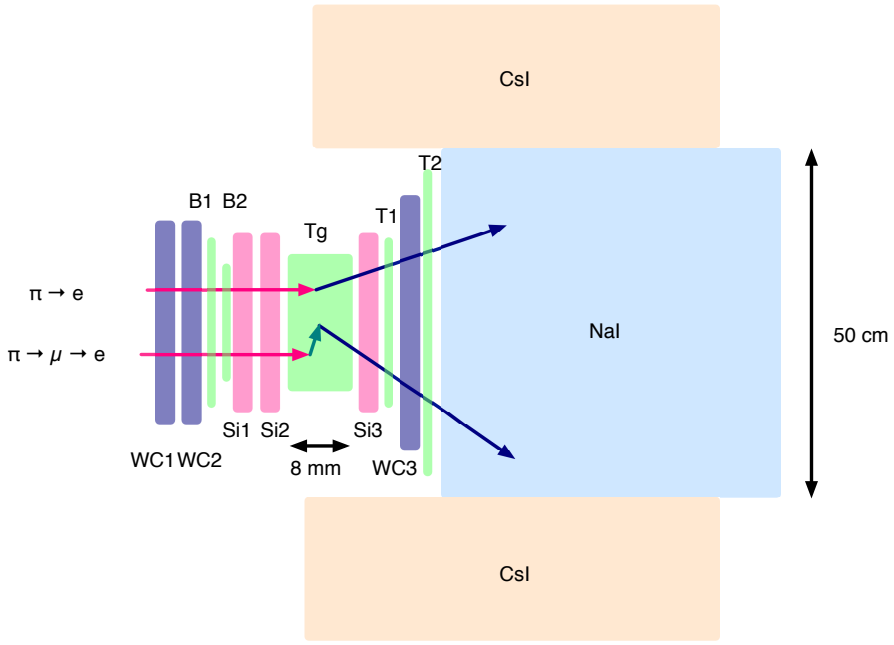

Figure 1.3: Schematics of the PIENU detector

1.2.2 Detector Setup

Figure 1.3 shows the detector arrangement. A 75 MeV/c π^+ beam from the TRIUMF M13 channel is identified by two beam counters (B1, B2) and stopped in an active scintillator target (Tg). Beam tracking is provided by two wire chambers (WC1, WC2), and two Si detectors (Si1, Si2) located immediately upstream of the Tg. The postrons' energy deposits and tracking from $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay and $\pi \rightarrow \mu \rightarrow e$ decays are measured in the positron telescope counters. They consist of a Si detector (Si3), two thin plastic counters (T1, T2), a third acceptance-defining wire chamber (WC3) in front of a NaI(Tl) crystal surrounded by pure CsI carolimeters. The analog signals of plastic scintillators are recorded by the COPPER 500 MHz Flash Analog-to-Digital-Converters (FADCs) which is described in the next chapter. while Si, NaI, and CsI detectors are recorded by VF48 60 MHz FADCs. And them, time informations are recorded by VT48 1.6 GHz Time-to-Digital-Comberters.

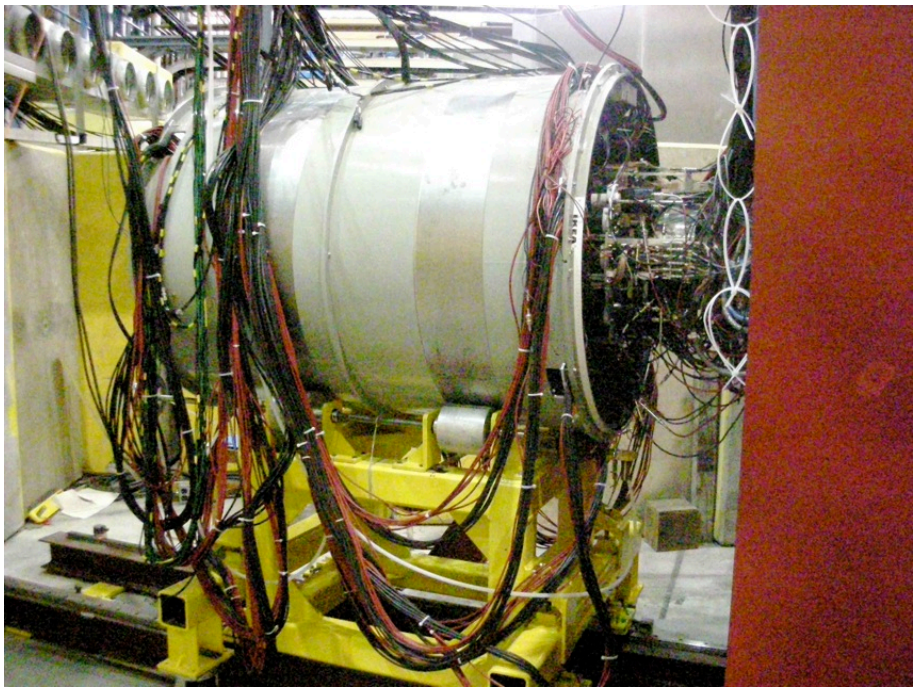

Figure 1.4: PIENU detector.

1.2.3 Beam Line

The TRIUMF M13 channel had upgraded to suppress the beam positron. In order to obtain a maximum acceptance, the detector system incloding large NaI(Tl) single crystal with CsI crystals arround it are placed on the beam axis. For the detector on the beam axis, the positrons in the beam severely increase the trigger rate and backgrounds in the positron time spectra. The beam line was modified to achieve a pion/positron ratio of > 50 by adding new magnets and using a differential energy loss method[1].

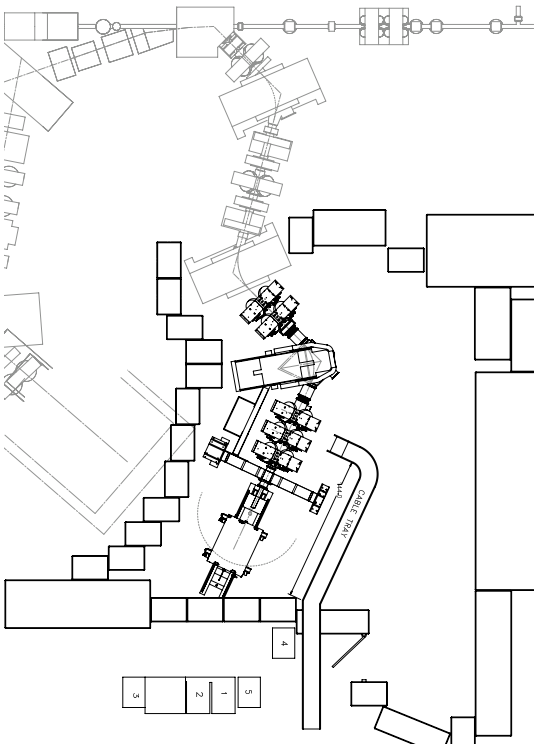

Figure 1.5: Schematics of M13 beam line. The black line shows reachable area.

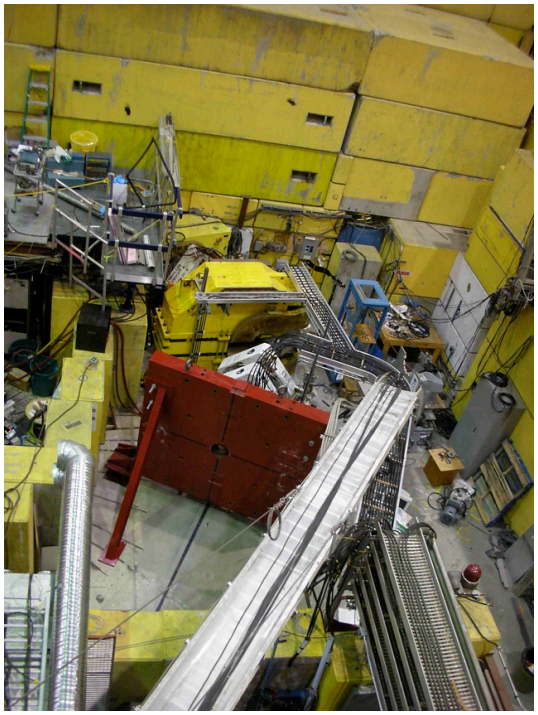

Figure 1.6: M13 beam line

1.2.4 Data Acquisition System

The PIENU Data Acquisition (DAQ) system consitsts of a NIM trigger logic, two type of FADCs and TDCs to collect large amount of $\pi^+ \to e^+ + \bar{\nu}_e$ events housing time and particle information. The timing information and waveforms are used to make the positron time spectra and identify the particles, respectively. Therefore the event building and synchronization between all modules are important in the DAQ system.

Obtaining all $\pi^+ \to \mu^+ + \bar{\nu}_\mu$ decay events severely increases the trigger rates, and then disturbs to increase $\pi^+ \to e^+ + \bar{\nu}_e$ statistics because the branching ratio of pion decays, $R = \Gamma(\pi^+ \to e^+ + \bar{\nu}_e)/\Gamma(\pi^+ \to \mu^+ + \bar{\nu}_\mu)$, is very small 10^{-4}. Therefore, to take the $\pi^+ \to e^+ + \bar{\nu}_e$ decay data with good efficiency and suppressing the $\pi^+ \to \mu^+ + \bar{\nu}_\mu$ decay data without bias are most important things in order to increase the statistics.

Trigger Logic

A trigger logic produces four different types of triggers to mainly take the $\pi^+ \to e^+ + \bar{\nu}_e$ data for statistics. This is based on conventional NIM modules.

At first, all physics triggers require the coincidence of the incident pion and the emitted positron. The timing of positrons are within -300 ns to 500 ns around the pion. The pion timing is defined by B1 $\cap$ B2 $\cap$ Tg while the positron timing is defined by T1 $\cap$ T2 counters, where $\cap$ stands for coincidence. The discriminator threshold of B1 also reject the beam positrons and muons which increase backgrounds

and trigger rates.

Sencond, the following four triggers were composed to collect $\pi^+ \to e^+ + \bar{\nu}_e$ events efficiently.

Pre-scale prescaled by a factor of 16,

Early requires the positron coming at the early timing (2 - 40 ns) after pion coming,

NaI-High requires high energy deposit (> 45 MeV) in the NaI calorimeter, and

CsI-Hit requires hits (> 5 MeV) in CsI crystals.

The Pre-scale trigger takes the normal data reduced by sixteen. The $\pi^+ \to \mu^+ + \bar{\nu}_\mu$ data severely increases the trigger rate, therefore it takes only 1/16 data. The purpose of Early, NaI-High, and CsI-Hit triggers is to take the $\pi^+ \to e^+ + \bar{\nu}_e$ decay data. Early trigger has a 40 ns narrow time window because pion life time is short and about 26 ns in contrast with muon life time is about 2.2 us. NaI-High and CsI-Hit triggers also have advantage to take $\pi^+ \to e^+ + \bar{\nu}_e$ data because the positron energy from $\pi^+ \to e^+ + \bar{\nu}_e$ ($T_{e^+} = 69.3$ MeV ($\pi \to e$)) is heigher than $\pi \to \mu \to e$ ($T_{e^+} = 0 - 52.3$ MeV ($\pi \to \mu \to e$)).

These triggers make the total trigger rate about 700 Hz. The $\pi^+ \to e^+ + \bar{\nu}_e$ rate is about 1 Hz, which is sufficient.

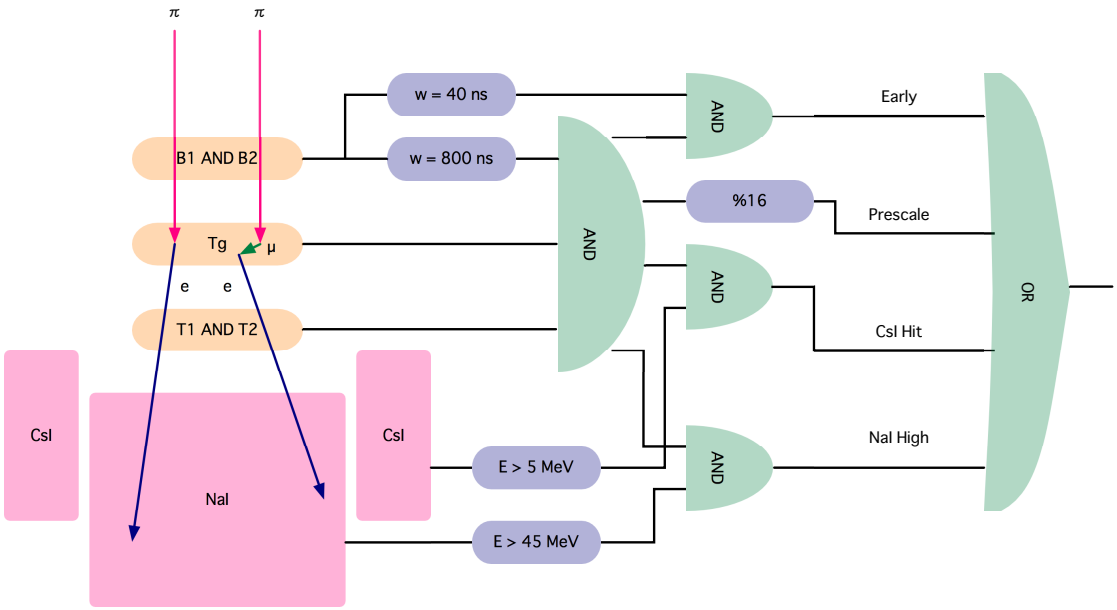

Figure 1.7: PIENU trigger diagram.

Waveform Digitizer

The PIENU experiment requires high rate waveform digitizers. The waveforms of the target scintillation counter are exceedingly useful to identify particles. And then, the identification of particles awfully

effects to measure the branching ratio. The pulse fitting method had been studyed and improved for the tagging decay modes[3][10].

This method aims to detect the second pulse delayed from the first pule. If the second pulse immediately comes, the second pulse may not be detected by the charges or pulse heights. Figure 1.8 shows the typical waveform of $\pi^+ \rightarrow \mu^+ + \bar{\nu}_\mu$ decay in the target scintillator. The template of particles is obtained from the single pulse data with TDC information. The following function is used for fitting waveforms assuming double pulses:

$$V(t) = A_1 F(t + T_1) + A_2 F(t + T_2). \tag{1.9}$$

F(t) is the waveform template for a single pulse and A_1, A_2, T_1, T_2 are the fitting parameters, the amplitude and timing of the first and second pulses, respectively.

Double pulses can be detected and rejected with almost 100% of efficiency when the second pulse is delayed by 2 ns or more from the first pulse. This separation is sufficient for the PIENU experiment.

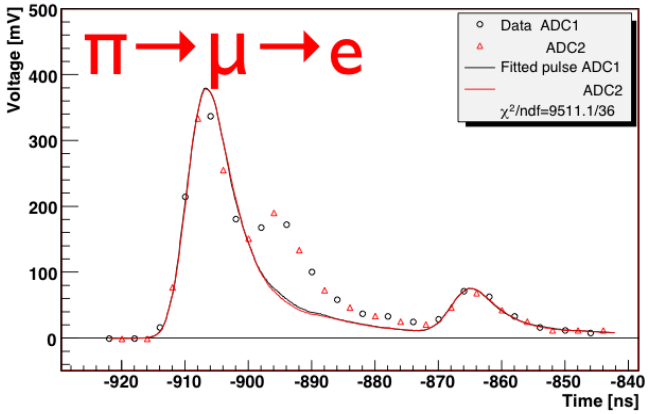

Figure 1.8: Typical wave form in the target

Requirements for FADC

One of the purposes to analyze the waveform in PIENU is to identify the particles. Another purpose is to monitor the muons which can cause the background The FADC system had modified to satisfy them [3] [8].

Synchronization of Multiple Channels Synchronizing the channels by the same clock is important to identify signal timings between many channels of the twenty PMTs connected with the five scintillators. The asynchronous channels can cause the pulse fit separations to be worth. The clocks, which drive electronic modules should be at the exactly same timing. A Clock Distributor module allows the COPPER 500-MHz FADC system to be drived by the synchronous clock and to sample the data.

Rejection of Pre-region Muons Buffering the past hits with long time window is also important to take the information of the beam muons before the trigger pions. The muons before the trigger pion should be sufficiently rejected because they can cause the backgrounds in positron time spectra by the

decay positrons. Figure 1.9 shows that the background in the positron timing distributions cut by the muon rejection. In order to reject them, the FADCs have to be able to take the data before triggers for about 6 μs. The firmware updates of the COPPER system was updated to achieve this goal[8].

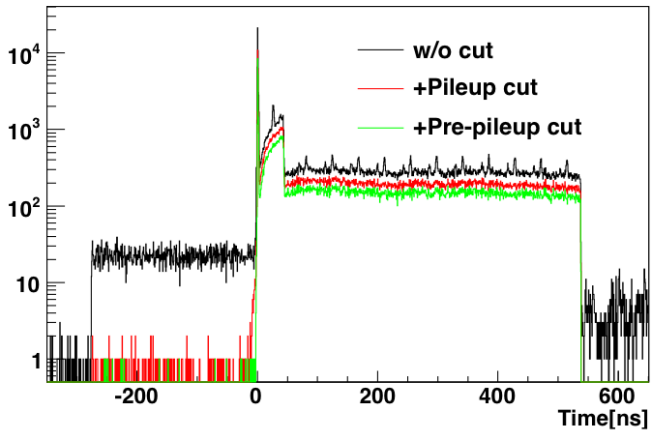

Figure 1.9: Positron timing distributions from pion decays. Black is the events withou cut. Green is the events without old muon.

1.3 Motivation of This Thesis

The COPPER 500-MHz FADC used by PIENU needed to be modified and updated in order to increase its reliability and usability. It was also required to adapt a new DAQ system which is planed to be installed in this spring. The modifications and upgrades of the COPPER 500-MHz FADC is described in this thesis.

1.3.1 Modification

The COPPER 500-MHz FADC used by PIENU had some problems to be modified for the reliability and usability. The problems from the firmware and hardware effected the synchronization of channels. Therefore, some modifications were required.

1.3.2 Upgrades

Upgrades of the DAQ system also required the firmware updates of COPPER. The trigger by the digital sum of calorimeter and asynchronous read-out system is installed. They enhanced the effective data rate. A time stamp and new trigger logic were required for the new function of DAQ.

1.3.3 Outline of This Thesis

Each chapters has the following contents. Chapter 1 describes the outline of the PIENU experiment. Chapter 2 describes the specifications and requirements of the COPPER 500-MHz system in PIENU.

Chapter 3 describes the modifications of a daughter card on the COPPER module to solve some problems. Chapter 4 describes adjustments of the COPPER system for the trigger and DAQ upgrades. At last, the summary is made in Chapter 5.

Chapter 2

COPPER 500-MHz Flash ADC System

2.1 COPPER 500-MHz Flash ADC System

The PIENU experiment is using a COmmon Pipelined Platform for Electronics Readout (COPPER) system[4] developed by KEK[6] to record the waveform of the scintillation counters. The COOPER 500-MHz FADC system for PIENU experiment consists of COPPER mother boards equipped with four daughter cards called FINESSE (Front-end INstrumentation Entity for Sub-detector Specific Electronics), a special VME crate modified for the COPPER specification, a Clock Distributor VME module and a General Purpose IO (GPIO) VME module. This section describes the basics of the COPPER 500-MHz FADC system for PIENU.

2.1.1 COPPER 500-MHz Flash ADC Module

Four COPPER mother boards are used in PIENU to record waveforms from the scintillation counters. Each COPPER mother board consists of four 500-MHz FADC FINESSE cards, where each card has two input channels. There are 8 channels in total for each COPPER mother board.

COPPER Mother Board

Each COPPER mother board consists of a processpr card, a trigger card, and four FINESSE cards. Table 2.1 shows some major specifications of the COPPER mother board. Figure 2.4 shows layout of the COPPER mother board.

The COPPER is a platform to compose many different types of FINESSE cards. The COPPER was designed with the following concept:

Front-End Buffering Signals from detectors are processed and buffered in individual FINESSE cards. When the buffered data are decided on recording for the analysis, they are transferred to the COPPER mother board. A trigger signal for the data transfer is accepted by the trigger card installed on the back-end of the COPPER mother board, and is uniformly distributed to four FINESSE cards. This is effective at reducing the dead-time since four FINESSE cards can work simulteneously.

Modular system The interface specification for the FINESSE card is well defined. Thus, the COPPER can be used as not only FADC but also TDC, ADC and so on by installing specific FINESSE cards. The trigger card can be also replaced with the other card if necessary. The interface for the

processor card is Generic PMC standard, thus any commercially-available processor cards can be used. This modular feature of the COPPER makes it flexible to design the total system, and also makes it easier to upgrade.

Programmable devices Most of the logics controlling COPPER mother board as well as FINESSE cards are implemented by Field Programmable Gate Arrays (FPGA). Therefore, it is rather easier to modify the system to fit the need of each experiment. One of major reasons why the COPPER system was employed by PIENU experiment is this easiness for the modification.

Table 2.1: Specifications of the COPPER mother board.

Size	9U euro card (KEK-VME)
Slots	4 $\times$ FINESSE card slots
	Processor PMC slot
	Trigger module slot
	General PMC board
Interfaces	VME-32 interface
	2 $\times$ Network interfaces
Others	32-bit 33 MHz PCI bus
	4 $\times$ 1 MB FIFOs

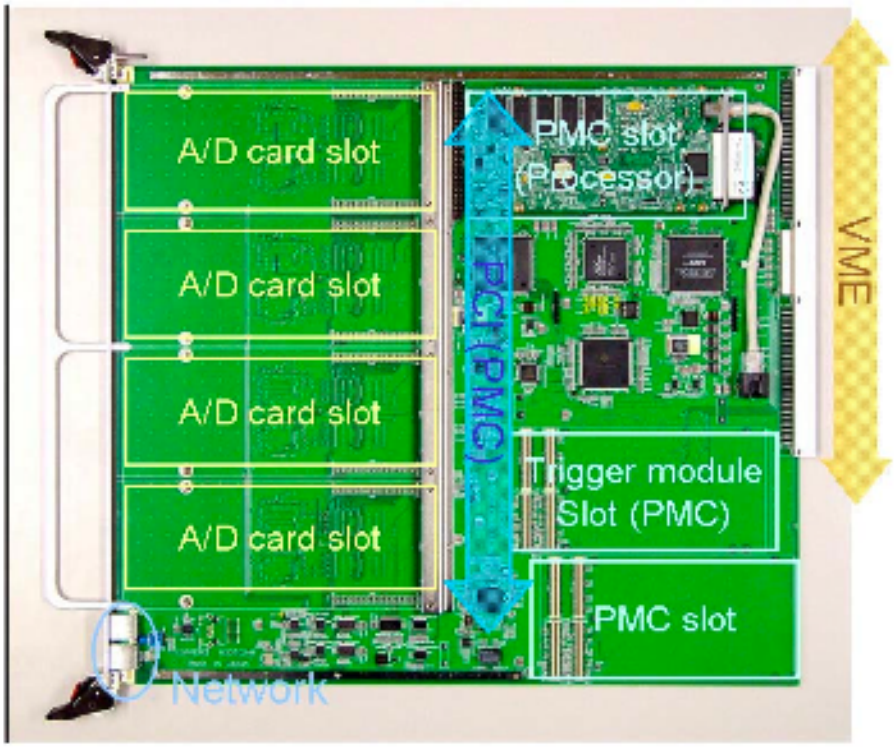

Figure 2.1: The layout of the COPPER mother board.

FINESSE 8-bit 500-MHz Flash ADC

PIENU experiment is using 8-bit 500-MHz FADC FINESSE card to record waveforms of the scintillator signals. The 500-MHz FADC FINESSE card is shown in Figure 2.2. The specification of the FINESSE

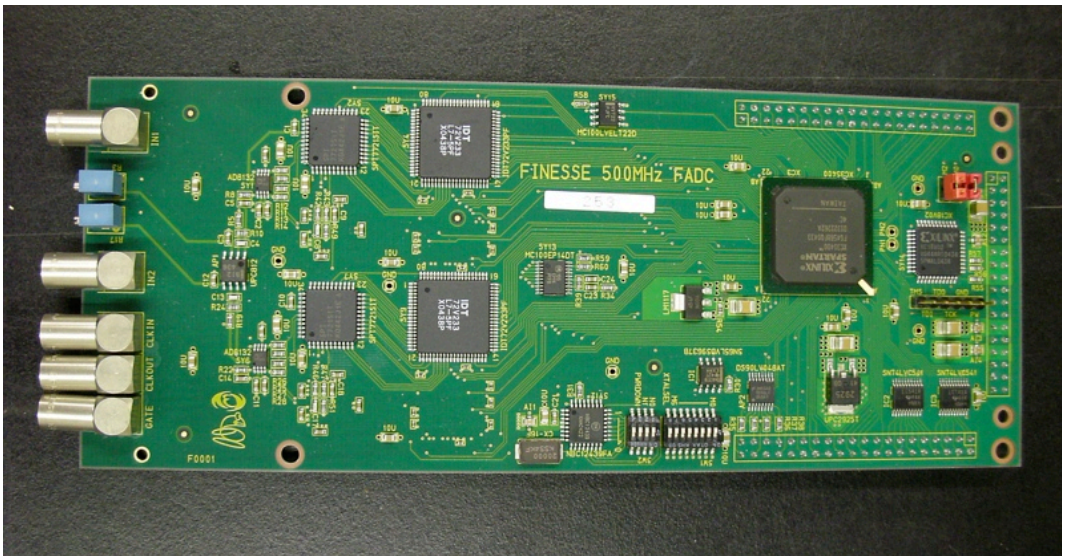

Figure 2.2: FINESSE 500-MHz FADC.

500-MHz FADC is summarized in Table 2.2. Table 2.3 shows model numbers and manufacturer of major ICs used in the 500-MHz FADC card.

The FADC card samples analog data in 500 MHz for about 8 μs. The waveform of a single channel is sampled by two ADCs driven by two 250-MHz clocks with alternate phases. The input dynamic range is ± 500 mV. The offset of input voltage can be adjusted by the screws in front of the card. The offset is set so that the dynamic range being from -950 mV to 50 mV. The resolution is 8 bits, and the effective number of bits (ENOB) is about 6.5 bits. The non-linearity of the FADC is less than 1%.

All ADCs and FIFOs on the card are controllded by FPGA, and the firmware of the FPGA can be modified if necessary.

Operation Scheme

Figure 2.3 shows schematic diagram of the data flow for 500-MHz FADC installed on the COPPER mother board.

The data flow can be divided to several steps. These steps are controlled by the FPGA. The clocks feeded to the FPGA are the 125 MHz to interface between FADC and FIFO and 42 MHz from the COPPER mother board. FPGA uses the 42 MHz clock to interface between FINESSE FIFO and COPPER mother board.

ADC Reset & Clock Synchronization The 125-MHz clock is produced by dividing 250-MHz clock in ADC. Thus, it is possible to have two different phases of 125-MHz clocks between different ADCs. The internal 125-MHz clock in a Clock Distributor module, which will be described later, is also produced by dividing 250-MHz master clock, and could have a different phase from the ADC on the

Table 2.2: Specifications of FINESSE 500-MHz FADC card.

Features	Descriptions
Main	8 bit resolution
	500 MHz sampling
	4 $\times$ 2.3 KB FIFOs
	FPGA operation
Inputs	2 ch analog signal
	250 MHz clock
	gate signal
Outputs	250 MHz clock
Dynamic range	-500 mV $\sim$ 500 mV
	2 $\times$ screws for offset

Table 2.3: IC chips used in the FINESSE 500-MHz FADC card.

ICs	Model Number	Manufacturer
ADC	SPT7721	FAIRCHILD
FIFO	72V233	IDT
FPGA	Spartan3 xc3s400 fg456	Xilinx
PROM	xc18v02	Xilinx

500-MHz FADC card. A reset signal is used to synchronize the phases of these 125-MHz clocks. The detail of the Clock Distributor and the reset signal are described later.

Writing Data to FIFOs ADCs pack two 8-bits data from the adjacent sample points into a single 16-bit word, and send the 16-bit word to FIFO with the 125-MHz write clock (WCLK) timing. FPGA controls write enable signals (WEN) for FIFOs so that the data from FADC can be recorded only during the gate input being asserted. In each 125-MHz clock timing, 32-bits words (4 sample points) coming from two ADCs are stored to FIFOs.

Buffering Data in FIFOs A binary counter in FPGA counts the number of words written to FIFOs. When the number of sampling points exceeds 1936, A read enable signals (REN) to FIFOs are asserted. Then, FIFOs start to drop their contents from the oldest word in every 125-MHz read clock (RCLK) while writting a new word to FIFOs in every 125-MHz WCLK. As a result, the number of words in FIFOs are kept at the same amount to hold waveform of the most recent 7.7 μs of time window.

Reading Data from FIFOs After closing the gate signal, if a trigger signal is provided to the trigger card, the trigger signals are distributed to each FINESSE cards. Then, FPGA switches its internal clock from 125-MHz to 42-MHz, and starts to move words in FIFOs to the COPPER mother board. Data from two channels are sent one after another.

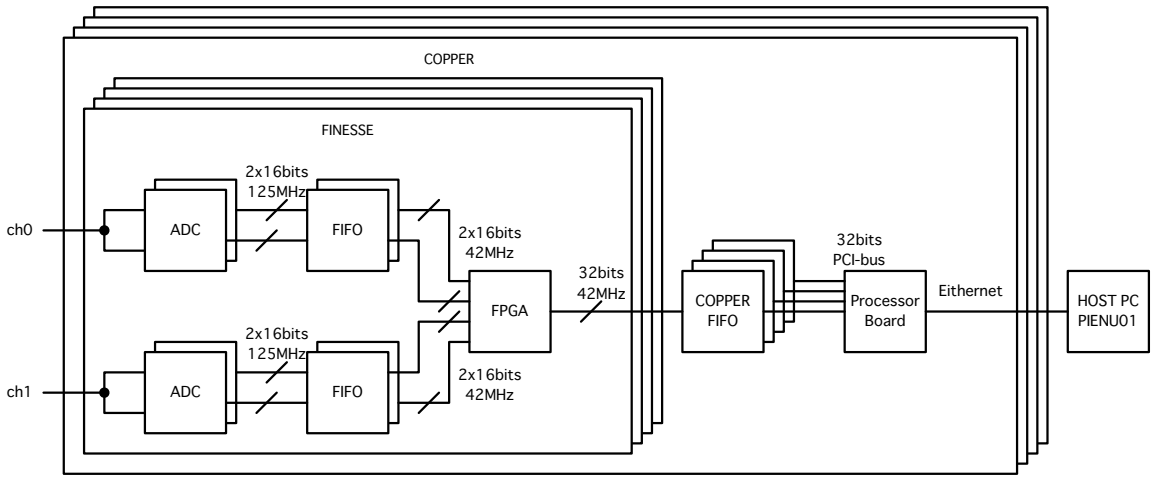

Figure 2.3: Schematic diagram of the data flow in FINESSE 500-MHz FADC.

Suppression of Data on the Processor The processor on the processor board catches the data transfer request from the yet another FIFO on the COPPER mother board after the completion of the data transfer between FINESSE and COPPER mother board. Then the processor transfer data stream to the internal memory through 32-bits PCI bus, and performs a data-size suppression to reduce the data size.

Sending Data to a Host Computer The suppressed data are sent to the host computer through the Ethernet. The processor board is booted on the compact flash. The booting procedure can be monitored through a serial cable if necessary.

2.1.2 KEK-VME Crate

All of the COPPER system modules are powered by the KEK-VME crate. The KEK-VME is the VME crate with KEK specific extension by adding J0 connector. The extension mainly aims to overcome a major weak point of the standard VME crate: insufficient power supplies for analog circuits. A new power supply unit with adequate currents for ± 3.3 V and -5 V are developed for the KEK-VME crate. A newly developed noise filter is equipped to achieve low noise environment for the analog circuit.

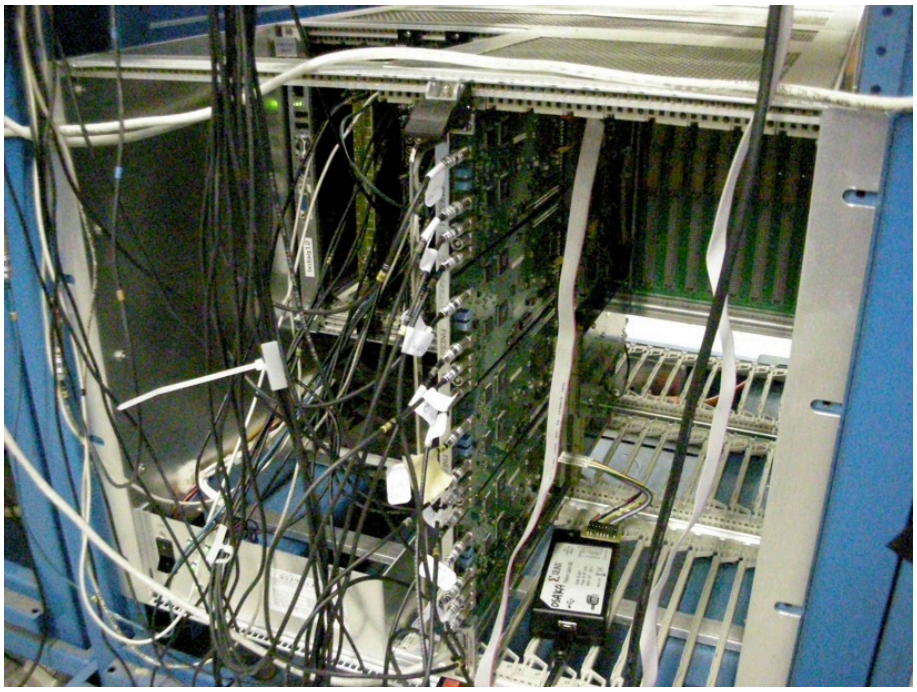

Figure 2.4: KEK-VME with the COPPER board

2.1.3 Clock Distributor Module

The Clock Distributor (CD) module is used to synchronize different channels of FINESSE cards. It also distributeslatched-gate signal and latched-reset signal as shown in Figure 2.6. The latched-gate and latched-reset signals with 125 MHz are nessesary to synchronize all channels. The programmable delays make it possible to adjust phases between the main clock and latched-gate and latched-resets.

The source of clock can be selected from external clock input and internal clock oscillator. This makes it possible to synchronize the clock between the COPPER system and the other modules by providing the master clock from the main logic system. Table 2.4 shows specifications of the CD module.

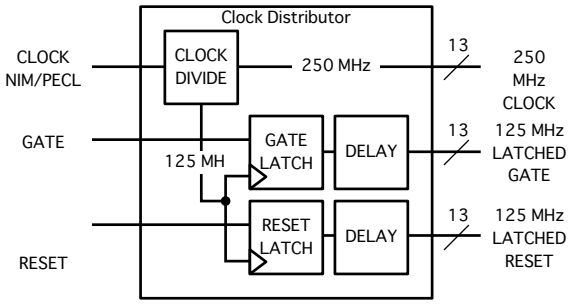

Figure 2.5: Schematic diagram of Clock Distributor.

Table 2.4: Specifications of the Clock Distributor.

Size	6U euro card (KEK-VME)
Inputs	1 $\times$ clock
	1 $\times$ gate
	1 $\times$ reset
Outputs	13 clocks
	13 $\times$ 125-MHz latched gates
	13$\times$ 125-MHz latched resets
Clocks	20 MHz NIM
	250 MHz PECL/ECL
	DIP switch
Others	CPLD operation

2.1.4 GPIO Module

A General Purpose Input Output (GPIO) module is a programmable logic with FPGA. It also provides several different I/O drivers which can be replaced by users. Figure 2.7 shows GPIO equipment with NUM I/O driver mode. A form factor of GPIO is 6U VME, and it has two driver card slots which can be chosen by the signal level you need. PIENU experiment is using it for the interface between COPPER system and a global trigger logic. Table 2.5 shows specifications of the GPIO module.

Table 2.5: Specification of GPIO.

Size	6U euro card (KEK-VME)
Main	25 MHz clock
	FPGA for logic operation
	CPLD for VME interface
Slots	2 $\times$ sub board slots
I / O	4 ch NIM signals
	ch ECL sub board
	16 ch NIM sub board
FPGA	Vertex xcv150 pq240 (Xilinx)
CPLD	xc9528 tq144 (Xilinx)

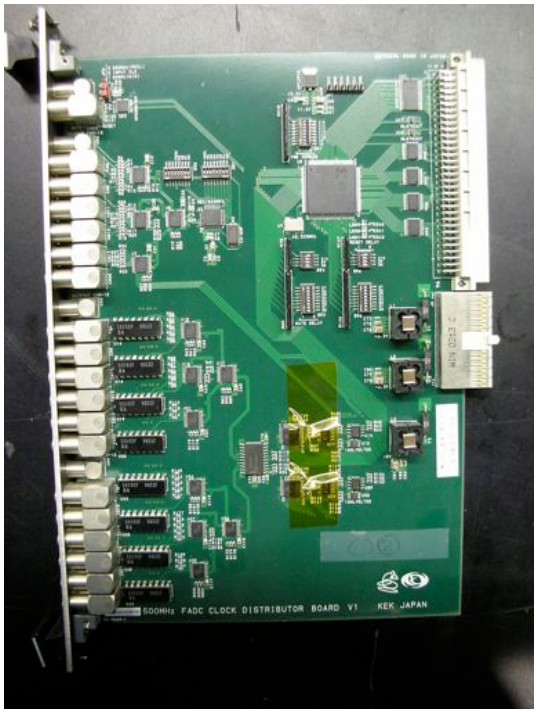

Figure 2.6: Clock Distributor.

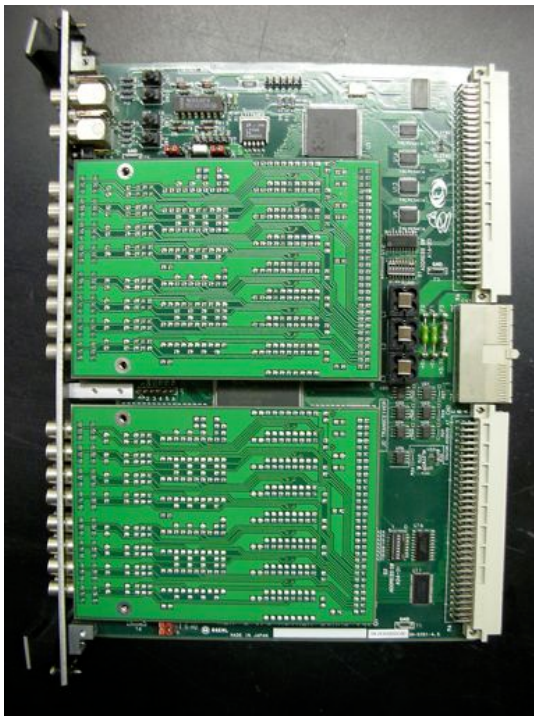

Figure 2.7: GPIO.

2.2 Synchronous Signal Setup

The synchronous signals were required for the check of ADC timing shifts. Not adjusting the Clock Distributor variables also caused the channel shifts. The difference of the time offset can be 8 ns when the clock, gate, or reset is not synchronized because all the FPGAs on FINESSEs are driven by 125 MHz clocks. Therefore, the CD module should be set and then the ADC timing shift data can be studied.

2.2.1 Setting of Gate Delay in CD

The PIENU experiment uses four COPPER modules with sixteen FINESSE cards. Each FINESSEs receives the synchronous clock, gate and reset signals from the CD module in Figure 2.8. However, to use only these is not enough to take the synchronous waveforms. The delay of the 125-MHz latched gates and resets should be properly adjusted by a few hundred pico seconds so that the latch timings in the FPGAs on sixteen FINESSEs should taken by the same edge of the clock. Figure 2.9 shows that the time window of the data is determined by the latched gate timing. If the edge of the gate is at the wrong position, the fluctuation of gate timing can cause 8 ns because the write clock (WCLK) is operated by the 125 MHz clock. Therefore, the gate to COPPER modules should be adjusted by changing the gate delay in the CD module. If the gate timing is not properly adjusted, the channel timing shifts can happen trigger by trigger.

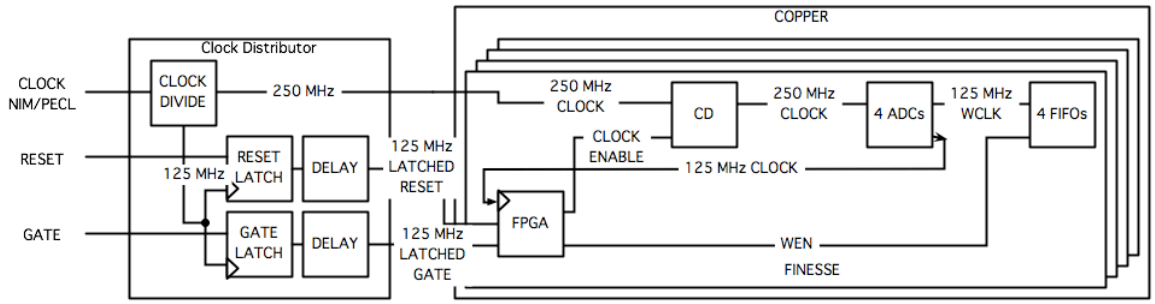

Figure 2.8: Diagram of connections between CD and COPPER to synchronize.

2.2.2 Setting of Reset Delay in CD

Figure 2.10 illustrates how the reset (RST) timing creates two phases of 125 MHz write clock (WCLK). The reset signal is latched by CD and sent to the FPGA on the FINESSE, and FPGA create the clock enable signal to the Clock Distributor (CD) chip with the preservative reset timing. The CD chip send the 250 MHz and inverse 250 MHz clocks to four ADCs, and then the ADCs make the 125 MHz clocks for data transfer.

The wrong reset timing can cause the channel timing shifts by 4ns (1 pt) between other FINESSEs or other runs. Since RST is sent to COPPER at the beginning of the run, the shift can happen FINESSE by FINESSE or run by run.

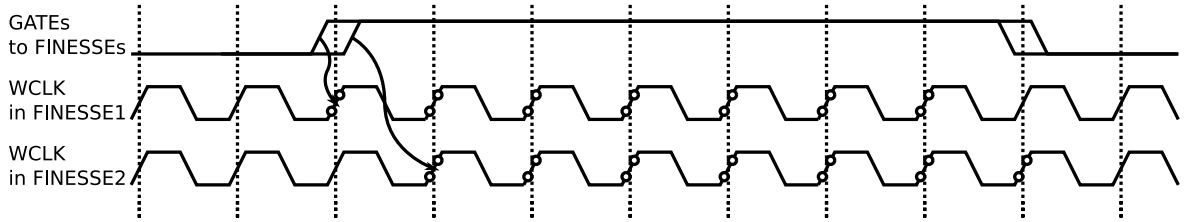

Figure 2.9: Diagram to determine the write enable (WEN) region by a gate signal (GATE). The data acquisition region could slip by 8ns because of 125 MHz operation clock (FPGA CLK) and WEN is created from GATE by FPGA CLK. The GATE timing cause different data acquisition regions by two point corresponding with 8 ns. This means each triggers' waveform can have different time offset without adjusting the timing between GATE and CLK.

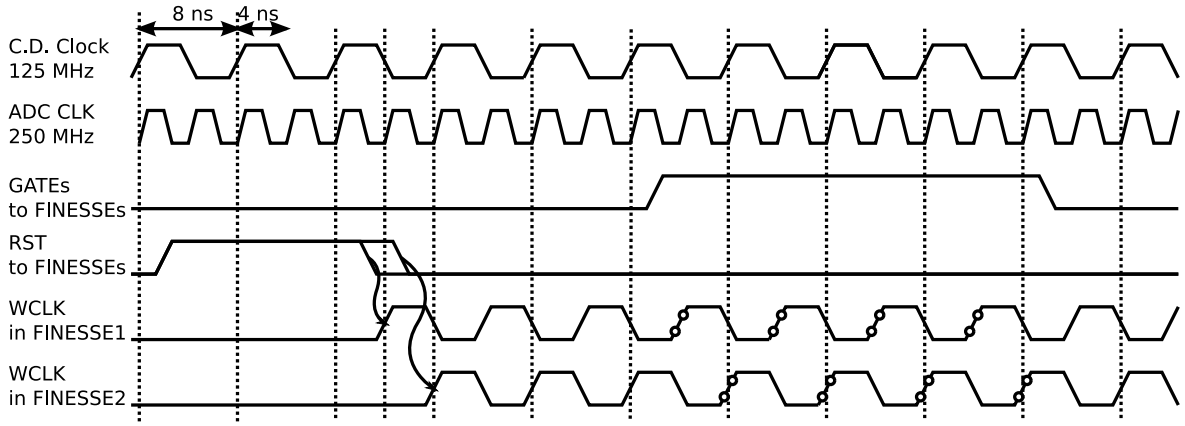

Figure 2.10: Diagram to determine the phase of 125 MHz write clock (WCLK) from ADCs to FIFOs by reset (RST). CD distributes 250 MHz clock (CLK) and 125 MHz latched RST. ADC divide the CLK to 125 MHz WCLK by RST timing. The two phases cause different data acquisition regions with same latched gate (GATE) by one point corresponding with 4 ns. This means two FINESSEs or two runs can have difference without adjusting the timing between GATE and CLK.

2.2.3 Logic for Synchronizing Test

The gate and reset variables of CD were adjusted for the test of ADC timing shifts and the PIENU DAQ system. Figure 2.11 shows the logic to set the CD module variables. When the firmware or the signal cable length is changed, the reset and gate delay values of CD have to be adjusted by using this logic.

A Function generator, GPIO or CD send the NIM 20 MHz or 25 MHz clocks, or PECL 250 MHz clocks to the CD to make the 250 MHz clocks to COPPERs. The synchronous signals are also sent to COPPERs as the analog input signals. The clocks of CD and the analog signals will be synchronized. These allow the synchronization of channels. Figure 2.12 shows typical waveforms used for the synchronizing test. By these, the ADC timing shifts can be detectable on the test bench and the PIENU setup.

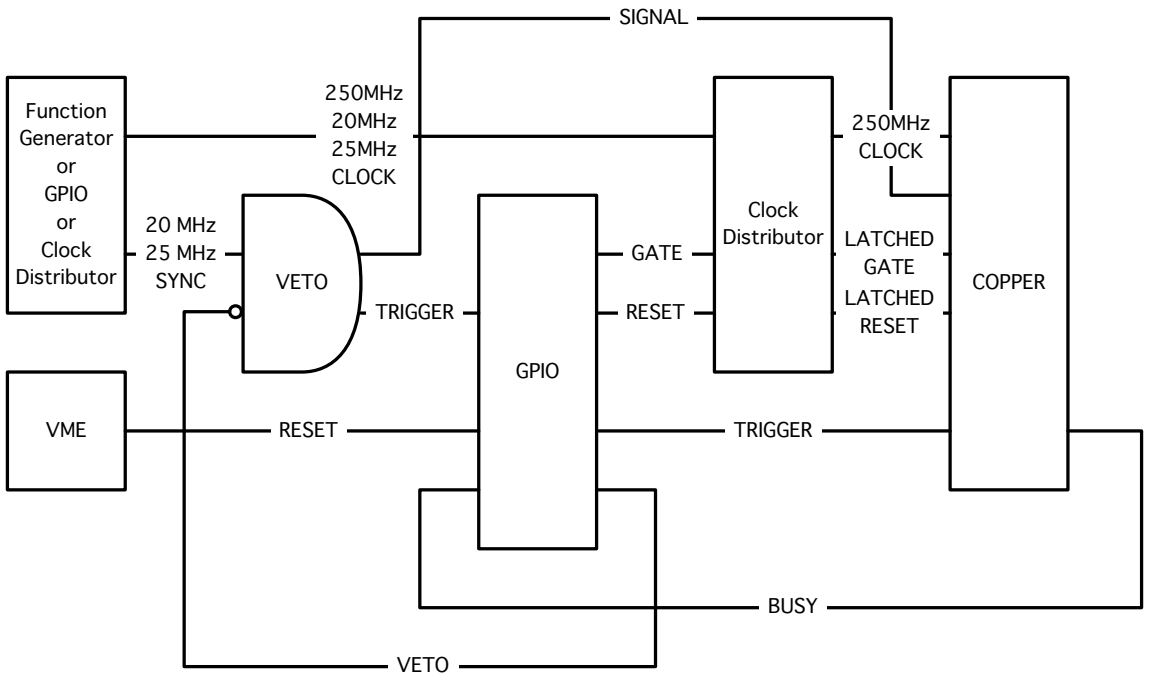

Figure 2.11: Logic diagram to make the synchronous signals. Function generator, GPIO, or Clock Distributor send the signals and the clock synchronized with each other. The signals, gates and resets into COPPER are synchronous because the clock synchronized with the signals creates the CD clocks, latched gates and resets.

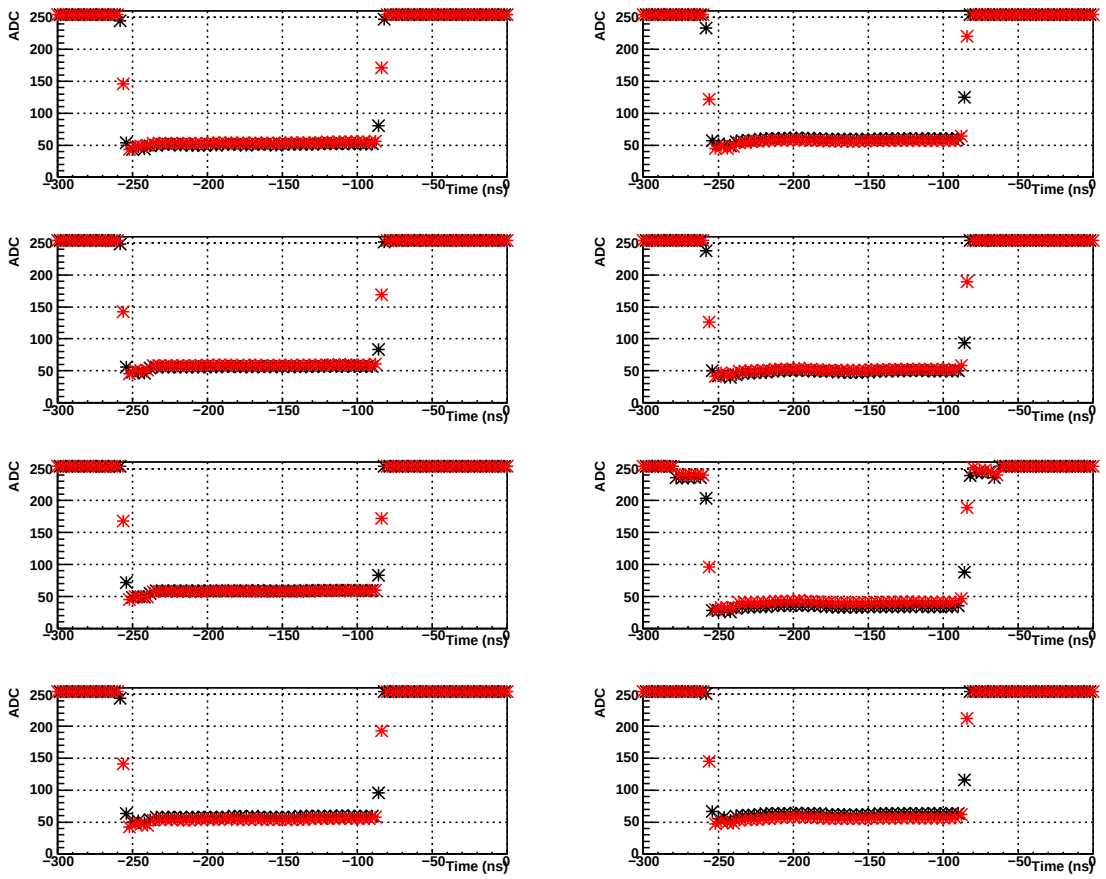

Figure 2.12: The waveforms of the synchronous signals. The synchronization of signals is checked by the timing just over the threshold.

Chapter 3

Modifications of FINESSE 500 MHz FADC

3.1 Issues of FINESSE 500 MHz FADC

There were three issues that would potentially spoil the quality of the FADC data. These are:

- Shift of ADC timing,
- Fluctuation of the number of sample points,
- Small margin of reset timing.

The Shift of ADC timing was caused by the failure of the synchronization between the drive clock for FADC and the control signal from FPGA. The fluctuation of the number of sample points could be caused by data missing due to miscount of data length for the buffering. The small margin of reset timing was caused by uneven length of signal lines on the COPPER mother board. The firmware updates of the FINESSE 500-MHz FADC solved these issues including a hardware issue. This section describes the details of these issues and solutions to them.

3.2 Shift of ADC timing

The shift of ADC timing happened when one of two ADCs in the same channel is driven by out-of-the-phase clock. This shift is detectable by monitoring the FIFO Empty Flag (EF) status event by event. With monitoring the Empty Flag, the timing of singals in FPGA was adjusted. This section describes the modification of the shift of ADC timing by a firmware update.

3.2.1 Issue

The FINESSE 500-MHz FADC realizes the 500 MHz of sampling freaquency by operationg two 250 MHz ADCs with 180° different phases of clocks. Figure 3.1 shows an example of the shift of ADC timing. The difference of the ADC time offset is 8 ns because the ADCs, FIFOs, and FPGA are driven by the 125 MHz as shown in Figure 3.2. The probability of seeing such shifts varies FINESSE card by FINESSE card.

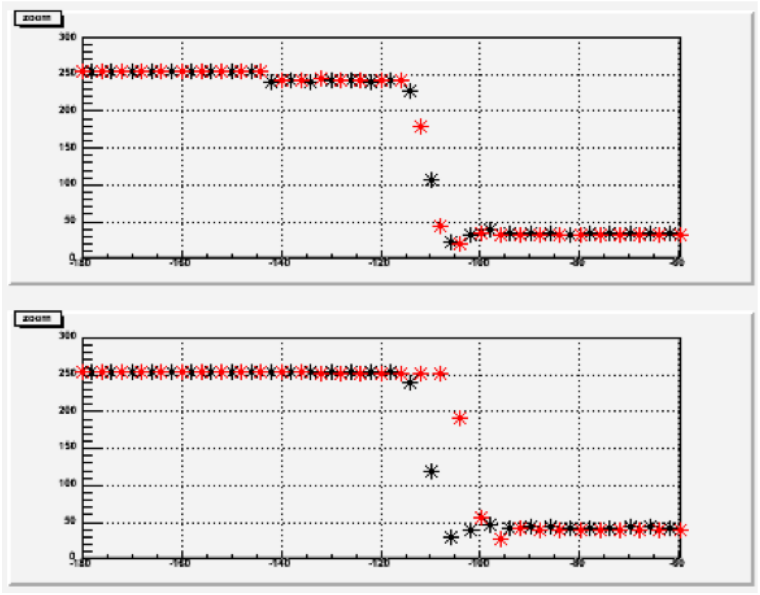

Figure 3.1: Waveform with time offset shift between two ADCs. Black points are the samples from one ADC, and Red points are the samples from another ADC. One ADC is shifted by two points (8 ns) because the data is sent by 125 MHz from ADCs to FIFOs.

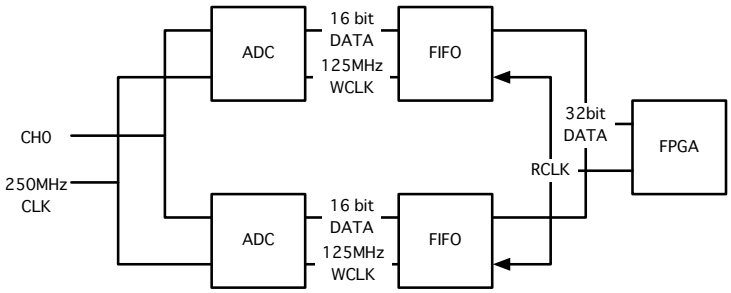

Figure 3.2: Schematics of one channel data from two ADCs and two FIFOs.

Endcode

In order to detect the potential ADC shift caused by the timing mismatch between the control signal from FPGA and the FADC clock, Empty Flag (EF) bits of each FIFO are recorded for the last two words. These bits are called endcode here after. The endcode consists of the EF status for the last two data transfered from FIFO to FPGA. Since each FINESSEs has four FIFO chips, the size of the endcode is 8 bits per event for a FINESSE card. Figure 3.4 shows a definition of the endcode. The 0xff is the normal endcode which means the last two data from all FIFOs The endcode except for 0xff alarms the endcode error. For the endcode values 0xaf and 0x5f should be corrected by shiftting the timing if one data missing in a FIFO is caused by one mechanism such as a missing of the write enable (WEN) or write clock (WCLK) for writing data on FIFO. However, during the engineering run, the existence of some events whose endcode could not correct the ADC timing perfectly was observed.

The FINESSE with the previous firmware was checked by the endcode and the synchronous signal tests. The half of FINESSEs were not available for the endcode error and a few FINESSEs caused hung-ups of the COPPER DAQ. The other strange phenomena is the compatibilities between particular FINESSE card and the position of FINESSE slot on the mother board. Some FINESSEs showed no error on a slot even if they showed errors on the other slots.

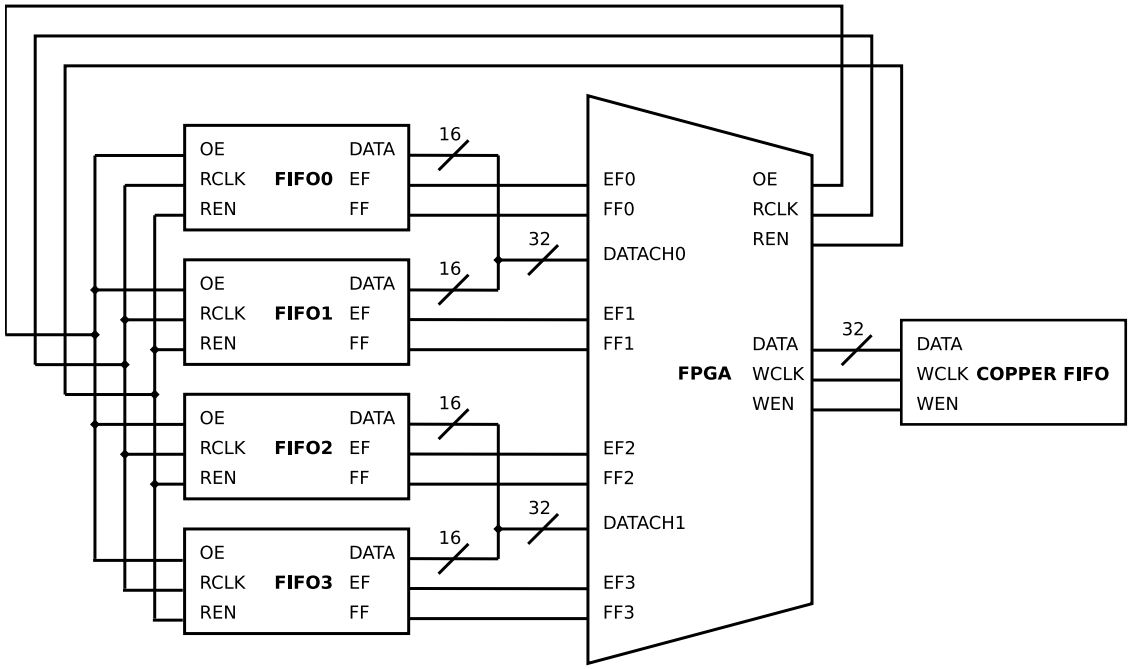

Figure 3.3: Diagram to read and write the data from FINESSE FIFOs to COPPER FIFOs. The empty flags create the endcode.

Temperature Dependence

Since the source of the endcode error was suspected to be a timing fluctuation between control signal and clock, the failure rate may depend on the system temperature. The temperature dependence of the

0xff					0xaf					0x5f					0x55				
data	FIFO0	FIFO1	FIFO2	FIFO3	data	FIFO0	FIFO1	FIFO2	FIFO3	data	FIFO0	FIFO1	FIFO2	FIFO3	data	FIFO0	FIFO1	FIFO2	FIFO3
last - 1	1	1	1	1	last - 1	1	1	1	1	last - 1	1	1	1	1	last - 1	0	0	1	1
last	1	1	1	1	last	1	1	0	0	last	0	0	1	1	last	0	0	1	1
last + 1	0	0	0	0	last + 1	0	0	0	0	last + 1	0	0	0	0	last + 1	0	0	0	0

Figure 3.4: Scheme to create the endcode. The endcode is made from the empty flag of last two data on FIFOs. FINESSEs have four FIFOs, so the endcode have 8 bits.

failure rate was studied by using the data from the engineering run taken between 27th July 2009 to 2nd August 2009.

Figure 3.5 shows the correlation between the temperature measured at the rack for modules and the endcode error from the FINESSE which has most frequent errors. Since typical number of events for a single run is 4×10^5, the probability of the endcode error is only 10^{-4}/event if the temperature is less than 29 degree.

The observed relation between the temperature and the endcode errors strongly suggest the instability of the FPGA signal timing. This is very strange since the commercial products such as the FPGA we are using should be very stable to the change of temperature unless the product could not be sold to public consumers. Some misusage of the FPGA logic was doubted.

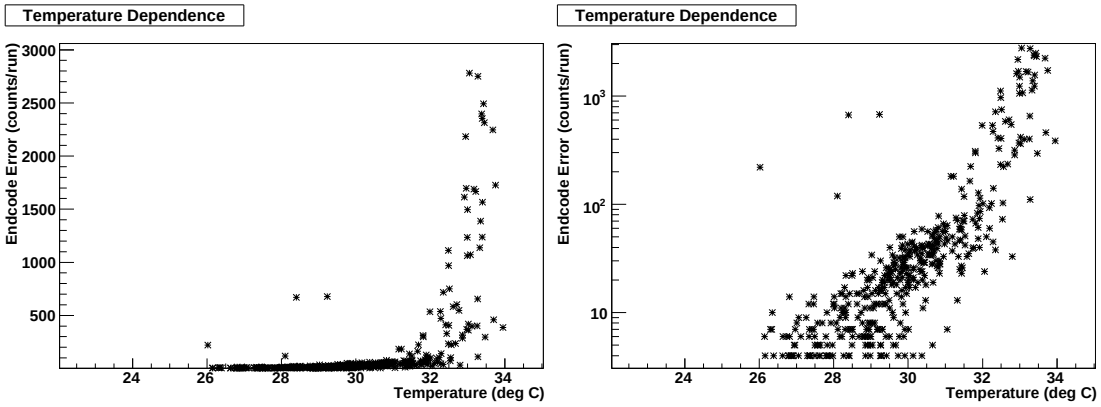

Figure 3.5: Endcode Error versus Temperature in the electronics rack. A strong correlation between endcode error and temperature exists.

Bias Check

The fraction of data set that have to be dropped due to the endcode error was 10^{-7}-10^{-2}. If the process of producing the endcode error was purely random, and does not have any correlation with signal amplitudes, then there is no problem. However, if there are any correlations, it would produce the systematic bias to the result of physics analysis when we drop the event with endcode errors. One of variables that could produce serious offsets is the amplitude of calorimeter because the positrons from $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ loss the high momentum in the calorimeter. Therefore, the triggers, including NaI calorimeter high trigger had investigated. The analysis with NaI spectrum was also performed.

Table 3.2.1 shows amount of the number of triggers and the ratio to all trigger data. Early and NaI_High contains larger amount of $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay events than PreScale. Figure 3.6 shows the ratio between the normal data and the data with endcode errors. They were consitstent within the statistical errors.

Table 3.1: Bias test by trigger. All physics triggers show no bias by the endcode errors

Trigger	Counts Without Error	Counts With Error	Ratio	Error	Error (%)
All	1.09741e+07	83121	0.007574	0.000026	0.35%
Early	2.32829e+06	17659	0.007584	0.000057	0.76%
NaI_High	3.26227e+06	24626	0.007548	0.000048	0.64%
PreScale	3.53905e+06	26841	0.007584	0.000046	0.61%

Figure 3.7 shows the energy spectrum of NaI. The top plots show the spectra over the threshold which is decided by Michel edge. The bottom plots show the spectra under the threshold. The edge around 18000 is defined by the NaI_High trigger. Therefore, this analysis have higher threshold than NaI_High trigger. If the amplitude of NaI signals causes the bias between the events with and without endcode errors, This analysis of the events could be sensitive to the effects to $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay. Table 3.2 shows the ratio of the number shown in Figure 3.7. NaI_PIE means the top histograms and NaI_PIMU is the bottom histograms. From this analysis, the bias was not seen within the systematics error.

Table 3.2: Bias test by NaI analysis. The analysis of positron energy shows no bias.

Trigger	Counts Without Error	Counts With Error	Ratio	Error	Error (%)
All	1.09741e+07	83121	0.007574	0.000026	0.35%
NaI_PIE	1.31598e+06	10049	0.007636	0.000076	1.00%
NaI_PIMU	9.93420e+06	75215	0.007571	0.000027	0.37%

The precision of the pion decay branching ratio that PIENU experiment aims to achieve is less than 0.1%, therefore the errors are required to be less than 0.1%. The trigger estimations achieved 0.0057% and NaI brief analysis achieved 0.0076%.

The biases coming from the endcode error are not observed in both trigger balance and the positron spectrum. However, this analysis was performed for a part of FINESSE cards and not all of them. There is no guarantees of the bias-free in data that will be taken in future. Thus, this study is far from

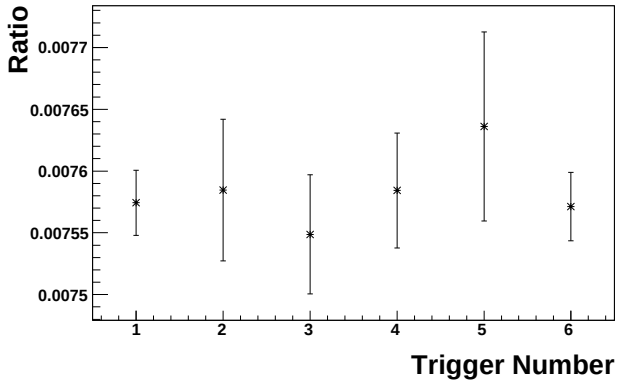

Figure 3.6: The difference between the triggers with and without the endcode error. 1: All, 2: Early, 3: NaIHigh, 4: PreScale, 5: NaI_PIE, 6: NaI_PIMU.

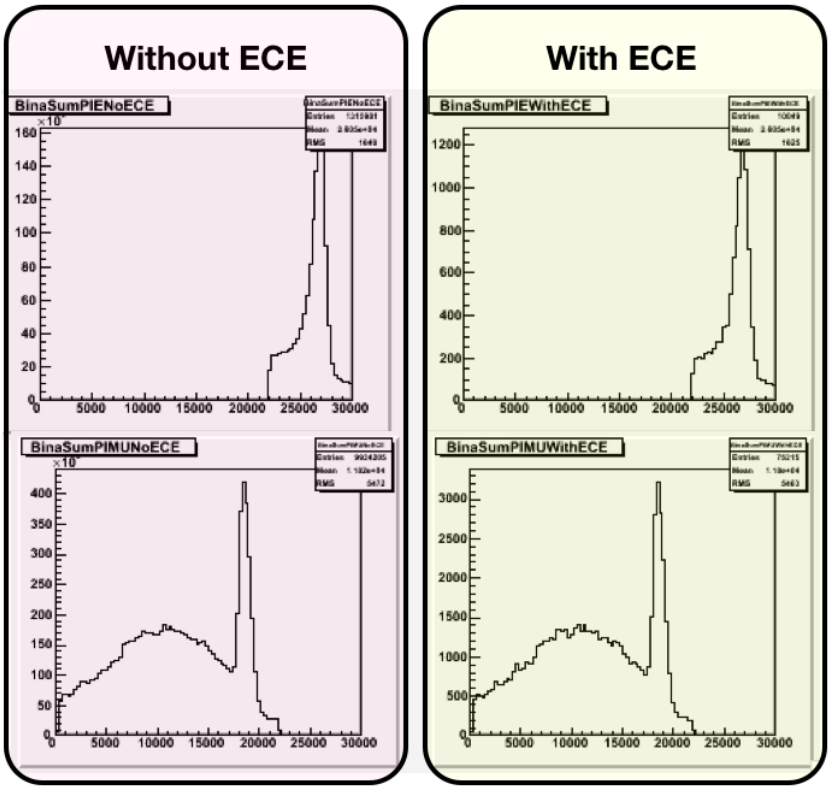

Figure 3.7: Positron energy spectra in NaI with and without endcode errors. Left and right histograms are without and with endcode error, respectively. Upper and down histograms mainly consists of $\pi \rightarrow e$ and $\pi \rightarrow \mu \rightarrow e$ decay positrons, respectively.

the comprehensive one, and the reliability of the 500-MHz FADC FINESSE card should be improved to reduce the rate of the endcode error.

Timing of Write Enable Signal

The shift of ADC timing can be suspected for some signal timings. The timing between the write enable signals (WENs) and the write clocks (WCLKs) was strongly suspected for the shifts. Figure 3.8 shows the connections of data and control signals between ADCs, FIFOs, and a FPGA while Figure 3.9 shows the timing of data writing on FIFOs Each FINESSEs has two channels (CH0, CH1). The ADCs provide the 125 MHz clocks (DCLKs) divided from the 250 MHz clock (CLK) to FIFOs with 16 bit data and the inverse DCLK (DCLKB) to a FPGA. In order to reduce the number of signal lines on the 500-MHz FADC card, the FPGA receives DCLKB only from ADC0. The FPGA creates the write enable signal0 (WEN0) for FIFO0 and FIFO2, and the WEN1 for FIFO1 and FIFO3 by the gate signal (GATE) and 125 MHz clock (DCLKB). Therefore, all the WEN signals which define the regions of data writing on FIFOs are driven at the rising or falling edges of DCLKB of ADC0. However, the phase of DCLK from ADC1 is 90 degree delayed from that of ADC0. The timing of WEN edge to the DCLK for ADC1 is different from that for ADC0 as shown in Figure 3.9. If the internal delays of signals in FPGA is changed by some reason such as temperature, WEN to some FIFOs might become off-timing from the WCLK edge and results in the missing words and the endcode errors. when the signals have some distortions by some changes such as temperatures.

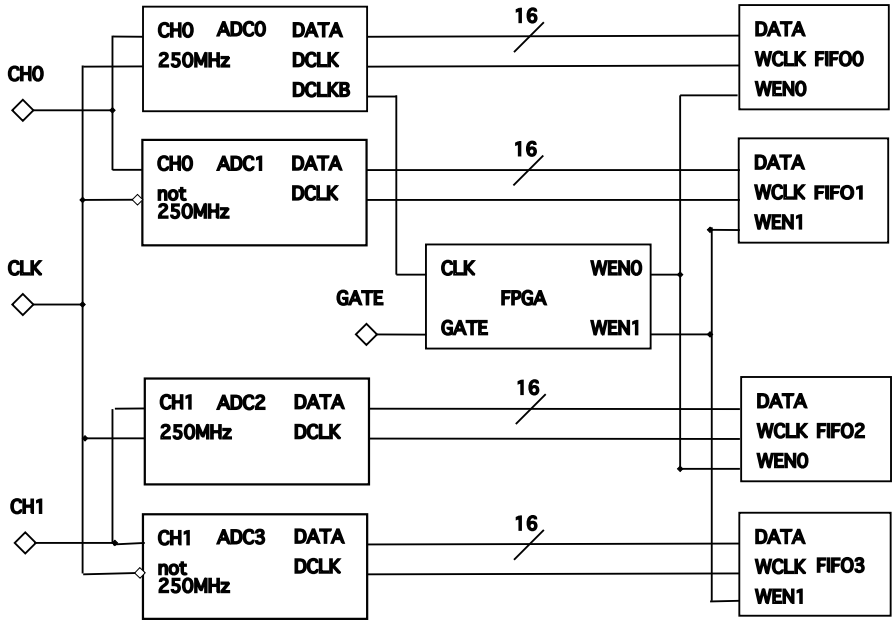

Figure 3.8: Schematics of two channel data from four ADCs and four FIFOs. Each channels has two ADCs and two FIFOs. The two ADCs send the data by the 125 MHz clock which is divided from 250 MHz themselves. The FPGA receives the one DCLKB which is divided to 125 MHz clock from 250 MHz clock through ADC0. It makes WEN0 and WEN1 from GATE with rising or falling edges of 125 MHz DCLKB. The FIFO0, 2 receive the WEN0 and FIFO1,3 receive the WEN1 signal to be written the data.

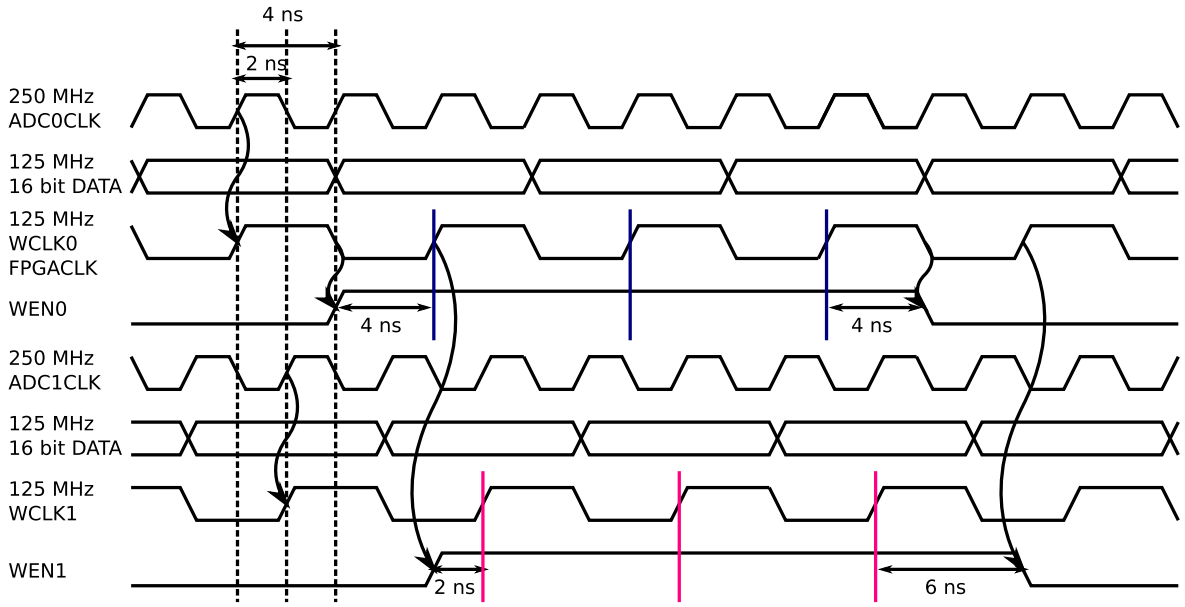

Figure 3.9: Timing chart to write one channel data on two FIFOs. Two ADCs for one channel are sampling with inverce 250 MHz clocks and sending with 90-deg shifted 125 MHz clocks. And the FPGA creates the write enable signal 0 (WEN0) for ADC0, 2 and WEN1 for ADC1, 3 from the gate signal. The FPGA latches the gate by the rising or falling edges of 125 MHz clock from ADC0 although the two 125 MHz clocks from the ADCs have 90 degrees difference. Therefore, some ADCs and FIFOs can have narrow margin. Blue line is the timing to write the ADC0, 2 data on FIFO0, 2 by WCLK0. Pink line is the timing to write the ADC1, 3 data on FIFO1, 3 by WCLK1.

3.2.2 Modification

In order to finely adjust the timing of WENs, the following functions of Xilinx FPGA were installed. The Xilinx FPGAs have the lines only for clocks and the Digital Clock Manager (DCM) function [9]. DCM is used for dividing clock or shifts of the clock phase. The new firmware changed the clock phase for REN, RCLK, and WEN. Figure 3.10 shows the hardware components on a Xilinx FPGA.

DCM The write clock needs to use the fine adjusted clock. The Digital Clock Manager (DCM) module provided by Xilinx can be useful. The module primitive in Xilinx FPGA parts is used to implement delay locked loop, digital frequency synthesizer, digital phase shifter, or a digital spread spectrum.

A Quadrant Phase Shift outputs shift the CLKIN input, each by a quarter period, as shown in 3.11. The CLK90 output is phase shifted $90\mathrm{deg}$ from the CLKIN input and so on. The both of 125 MHz clock and 42 MHz are driven by DCMs. The phase of the clocks is very important because the clocks make the timing of WEN, REN, and RCLK. The signal synchronizations was tested with all phases of the clocks by $90\mathrm{deg}$.

BUFGMUX The read clock (RCLK) have two different frequencies clocks, 42 MHz and 125 MHz to interface with COPPER and to drop for buffering, respectively. The Xilinx FPGA has BUFDMUX module, Global Clock Multiplexer (BUFGMUX) for multiplexing two clocks.

The BUFGMUX can multiplex between two clock sources or be used as a simple BUFG clock buffer as shown in Figure 3.12. Clock buffers / multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

The BUFGMUX not only multiplexes two clock signals but does it in a way that eliminates any timing hazards. This allows switching from one clock source to a completely asynchronous clock source without glitches in Table 3.3. The element guarantees that when the select line S is toggled to choose the other source, the output can be either High or Low when disabled (when toggling between clock inputs). A cross-coupled register pair ensures the BUFGMUX output does not inadvertently generate a clock edge. When the S input changes, the BUFGMUX does not drive the new input to the output until the previous clock input is Low-to-High transition of the input, the output clock pulse is never shorter than the shortest input clock pulse.

The installation of BUFGMUX allows the clocks to be clean. The clean RCLK waveform will not disturb to read the data.

Table 3.3: BUFGMUX.

Inputs			Outputs
I0	I1	S	O
I0	X	0	I0
X	I1	1	I1
X	X	$\uparrow$	0
X	X	$\downarrow$	0

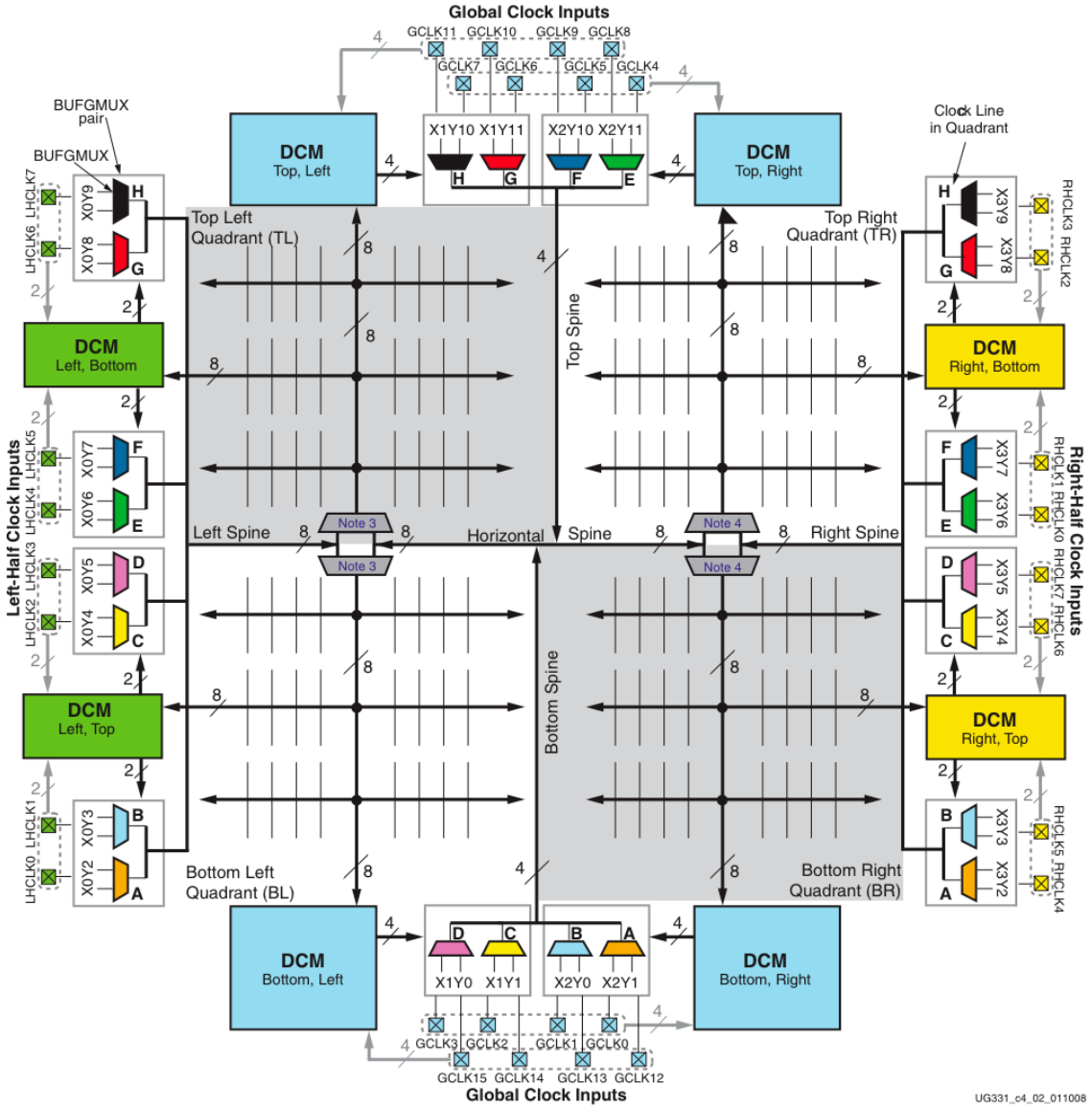

Figure 3.10: Diagram of signal lines and modules for clocks of Xilinx FPGA. Hardware DCM and MUX are located on near the edges of FPGA. Global clock line is also located over a FPGA.

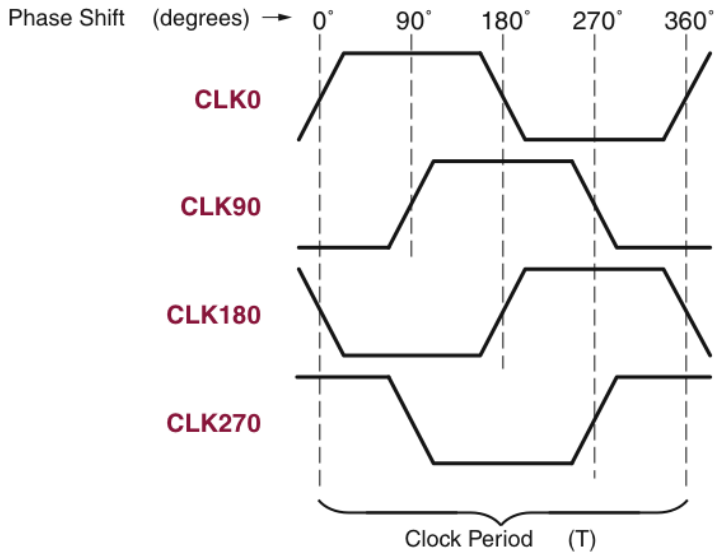

Figure 3.11: Quadrant Phase Shift Outputs Shift CLKIN, Each by a Quarter Period

UCF The clock frequency and other specifications of signals can be constrained in the User Constraints File (UCF). The constraints can affect how the logical design is implemented in FPGA, and it also affects the shape of signals, so it can not be ignored. There are several types of logical constraints in the UCF file.

Placement The placement of modules

Mapping The mapping signals to the pins

Timing The timing of signals to a clock

By these adjustments, the timing of signals could be modified. The FPGA uses the 42 MHz clock for the interface with COPPER and the 125 MHz clocks for the interface with the ADCs and FIFOs. The ucf file describes the two clocks are 42 MHz and 125 MHz. All skew is constrained less than the interval by these descriptions. The signal specification and the current to drive signals were also adjusted. The appropriate specification and enough current made the signals clean. The mapping lines related clocks also had been changed to avoid FPGA error. The installation of DCM and BUFGMUX exceeded the FPGA hardware limit. The FPGA doesn't have enough lines for clocks defined by the model. Therefore, a mapping of the line, which doesn't have not so large effects on timing was changed.

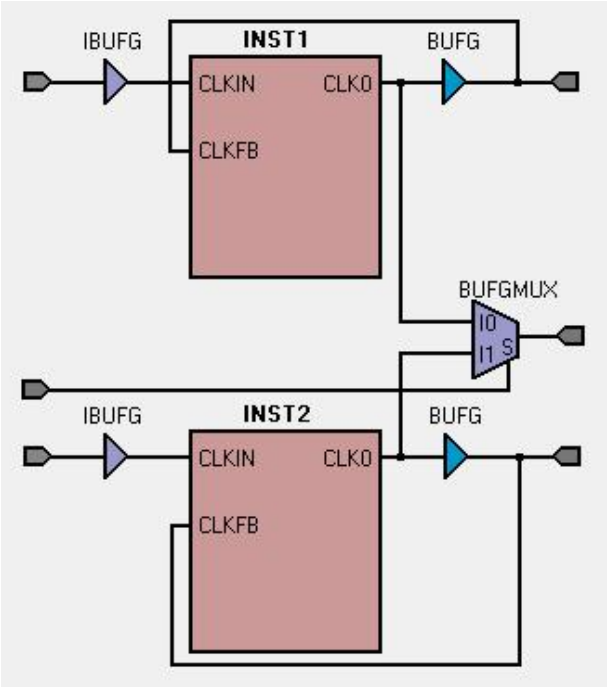

Figure 3.12: BUFGMUX.

3.2.3 Results

Figure 3.13 shows the RCLK for buffering. The shape and offset became stable by the updates of the firmware.

The previous firmware causes the endcode errors with the ADC shifts ($10^{-7} - 10^{-2}$) at the engineering run. The updated firmware results in no endcode errors ($< 10^{-9}$) for the enginering data taken with real beam. The bench test also showed no endcode error and no ADC timing shifts ($< 10^{-7}$) for four FINESSEs. The other 36 FINESSEs also have no endcode error and no shift of ADC timing ($< 10^{-6}$). Another effective result is all of the FINESSE became to be usefull. Those were not usable with the previous firmware.

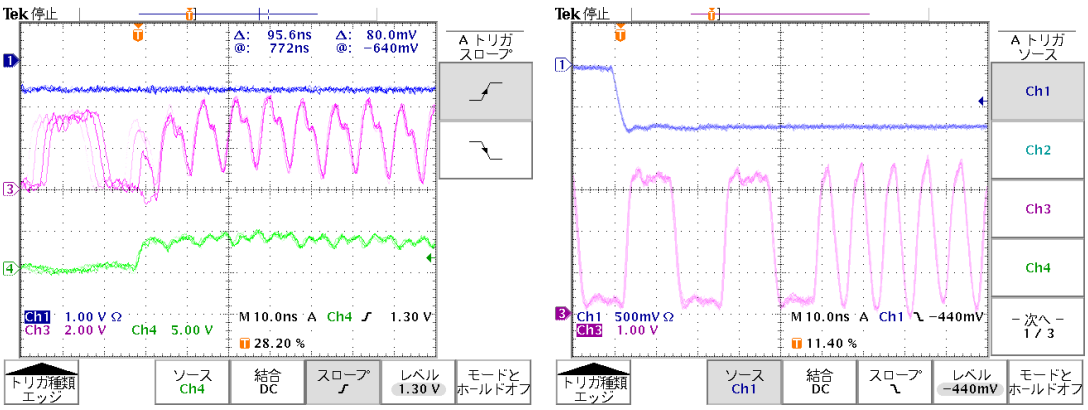

Figure 3.13: Left: Switch the read clock (RCLK) to the FIFO from 42 MHz to 125 MHz with normal MUX and not adjusted standard. Pink line is RCLK, and green one is an internal gate signal (GATE). GATE signal determines which clock is used for RCLK. RCLK is not so stable and have unstable offset when switched from 42 MHz to 125 MHz. Right: Switch the read clock (RCLK) to the FIFO from 42 MHz to 125 MHz with the MUX for clock and adjusted standard. Pink line is RCLK, and blue one is an external gate signal (GATE). GATE signal determines which clock is used for RCLK. RCLK is so stable when switched from 42 MHz to 125 MHz.

3.3 Fluctuation of Number of Sample Points

The modification was required for unstable number of sample points. The number of sample points is defined by the firmware of the FINESSE 500-MHz FADC. The number is counted when the gate is open, and the old sample points are dropped after the counter becomes 7.7 μs. All of the data which have more than 7.7 μs gate should have the same number of sample. The behaviors of number of sample points was investigated by synchronous signal tests. This section describes the modification of the fluctuation of number of sample points.

3.3.1 Issue

The number of sample points is controlled by the firmware of FPGA that controls all the functions of the 500-MHz FADC FINESSE card. A binary counter implemented in the FPGA counts the number of words stored to the FIFO. The counter starts when the gate signal is asserted, and the old data is dropped when the total number of words in the FIFO exceeds 975 words. Therefore, the number of words stored in the FIFO should be the same for all the FIFOs as long as the length of gate open is long enough. However, during the engineering run, the fluctuations of the number of words were observed. Figure 3.14 shows typical plot of the stability of the number of sample. The number of samples in two of four FINESSEs takes three values. The mean of the number of samples started from the larger value or the smaller value and is quickly changed to the middle number, but never became stable at a single value. This behavior was observed almost all of the 500-MHz FADC cards. Since the number of words in FIFO is controlled by REN and WEN, this observation strongly suggests that the timing of either REN or WEN or both is not stable. Since it is related to the REN and WEN timings, correlation with the shift of ADC timing was suspected. The shifts of ADC time offset also happened FINESSE by FINESSE with the fluctuation of number of samples. The origin of the shifts of time offset may be correlated with the number of sample. If the number of samples is stable, the value can be the monitor of the shift of ADC timing. It is also one of the motivations to modify the fluctuation.

Data Buffering

The time window of the waveform being recorded by the 500-MHz FADC is the latest 1936 sample points right before the trailing edge of the Gate signal. In order to realize this feature, REN for FIFO is controlled by FPGA so that the old words is dropped. Figure 3.15 shows block diagram of 500-MHz FADC card with data and control signals related to the buffering.

The buffering is operated by the write enable (WEN), write clock (WCLK), read enable signals (REN), read clock (RCLK), and FPGA internal counter (CNT) as shown in Figures 3.15 and 3.16. CNT to count the written data starts by the opened gate signals with 125 MHz clock. And then, the REN starts to dump the old data with 125 MHz 16 bit for each FIFOs after the CNT becomes the number to define the limit of data size. Figure 3.16 shows that REN starts to dump the data when CNT are 968×8 ns $= 7744$ ns. The read out rate is the same with the writing rate from the four ADCs. At last, the close timing of the gate stops WEN and REN. Therefore, the number of sample should be also the subtraction between the width of WEN and the width of REN. The latest 7.7 μs data are always in the FIFOs.

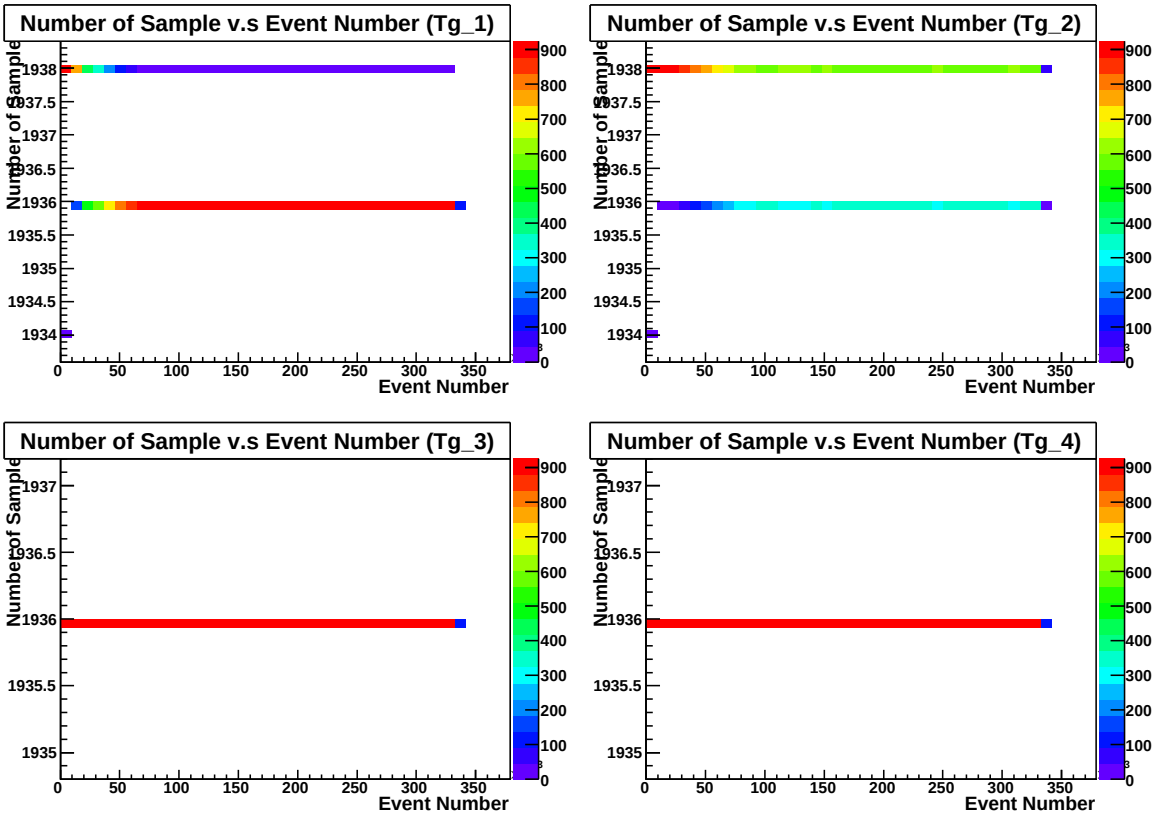

Figure 3.14: Number of sample versus event ID for four FINESSEs. Four FINESSE have three types of numbers of sample. The number 1936 seems to be stable.

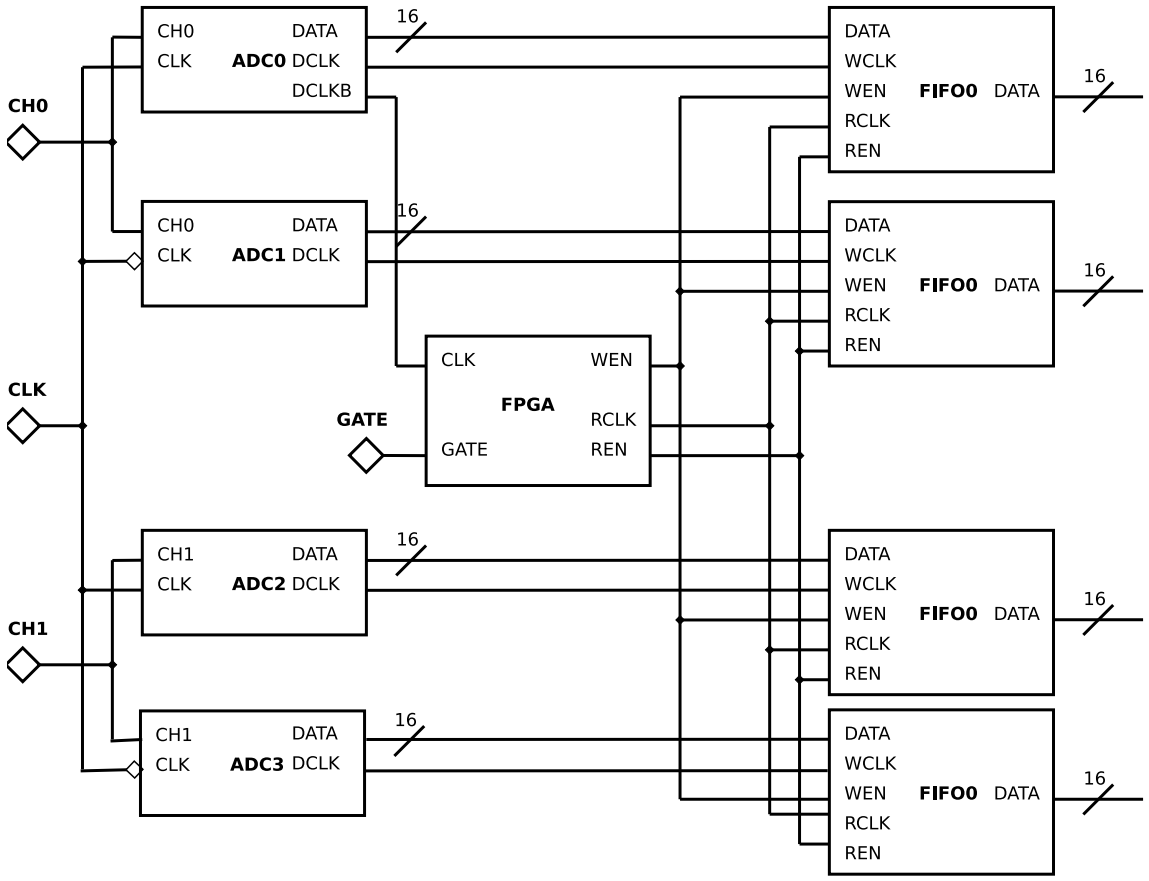

Figure 3.15: Diagram to send and dump the data. The FPGAs on each FINESSEs control the signals, and FIFOs buffer the data for 7.7 us.

Number of Sample with Synchronous Signals

The synchronizing channel test for the gate signal is performed to understand the behaviors. The delay of the 125-MHz latched gate signal by the Clock Distributor is scanned by 200 ps to monitor the edges and the number of sample. Figure 3.17 shows the number of sample with the scanned delays. It has about 5.4 ns margin from 2600 ps to 8000 ps within 8 ns for the four COPPERs. On the other hand, Figure 3.18 shows the edge timing of the synchronous signals with the scanned delays. It has about 3 ns from 3000 ps to 6000 ps within 8 ns for the four COPPERs. The numbers of sample have the different distribution in contrast to the synchronous signal edges. The gate time margin of the number of sample points is narrower than the edges. This means WEN and REN signals must be operated by different clocks. Figure 3.19 shows one of the number of samples shift hypothesis. The tiny difference between WEN and REN can cause the shift.

The gate for the synchronous edges should be stable at the end of the gate, but the gate for the number of sample should be stable at not only the end of the gate but also the beginning of the gate.

When the gate exists in the delicate region, the gate can cause the occational time offset shifts. In order to avoid the shift of the number of sample, the clocks to latch the gate for WEN, and to start and stop the counter for REN should be the same.

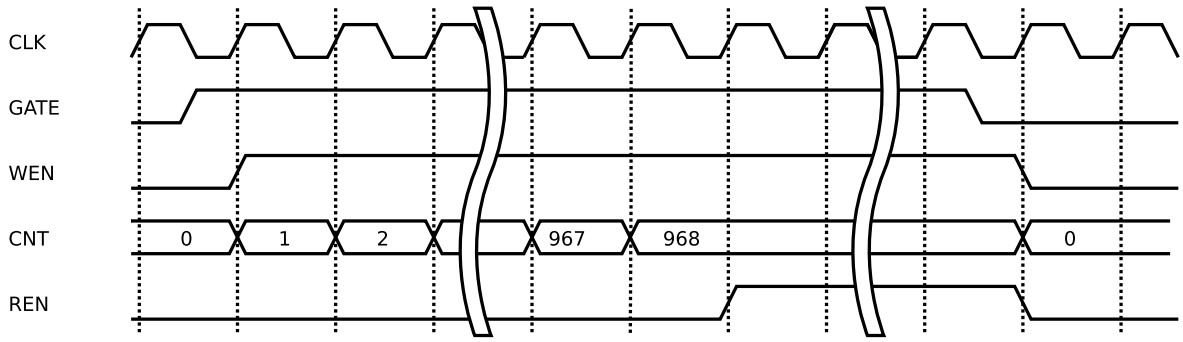

Figure 3.16: Logic diagram to buffer the data. Counter (CNT) starts to count clock signal (CLK) at the gate coming, and Read enable (REN) starts to dump the data when CNT becomes 968 corresponding with 7.7 us.

Number of Sample	c0				c1				c2				c3			
Gate Delay	f0	f1	f2	f3	f0	f1	f2	f3	f0	f1	f2	f3	f0	f1	f2	f3
0	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934	1934	1934.02
100	1934	1934.66	1934	1934	1934	1934	1934	1934.02	1935.78	1934	1934	1934	1935.46	1935.98	1935.98	1935.98
200	1935.98	1935.98	1935.98	1936.8	1937.7	1935.98	1935.98	1935.98	1936.66	1937.94	1937.94	1936.24	1936	1937.98	1938	1936.02
300	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936
400	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936
500	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936
600	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1936	1934.51	1934.62	1935.7
700	1934.02	1934.02	1934.02	1936	1936	1935.14	1936	1935.96	1934.02	1934.1	1936	1936	1934.02	1934.02	1934.02	1934.02
800	1934	1934	1934.02	1934.02	1934.02	1934.02	1934.02	1934.02	1934	1934	1934.02	1934.02	1934.02	1934	1934	1934
900	1935.98	1936.02	1934.16	1934	1934	1934	1934.04	1934	1935.98	1934.9	1934	1934	1935.98	1935.98	1935.98	1935.98

Figure 3.17: The number of sample at various gate delay settings through the previous firmware] The stable margin is about 3 ns from 3000 ps 6000 ps for 1 kevents.

Signal Edge Timing	c0				c1				c2				c3			
Gate Delay	f0	f1	f2	f3	f0	f1	f2	f3	f0	f1	f2	f3	f0	f1	f2	f3
200	80.99	80.99	80.99	82.99	80.99	80.99	80.99	80.99	80.99	80.99	81.99	85.99	80.99	81	80.99	80.99
220	81	81	80.99	82.99	80.99	80.99	80.99	80.99	81	80.99	81.99	85.99	80.99	81	81	81
240	81	81	81	82.99	80.99	81	80.99	80.99	81	81	82	85.99	81	81	81	81
260	81	81	81	83	81	81	81	81	81	81	82	86	81	81	81	81
280	81	81	81	83	81	81	81	81	81	81	82	86	81	81	81	81
300	81	81	81	83	81	81	81	81	81	81	82	86	81	81	81	81
800	81	81	81	83	81	81	81	81	81	81	82	86	81	81	81	81
820	81	81	81	83	81	81	81	81	81	81	82	86	81	81.35	81	81
840	81	81	81	83	81	81	81	81	81	81	82	86	81	82.88	82.7	81.2
860	81	81.09	81	83	81	81	81	81	81.63	81	82	86	81.54			
880	82.45	82.74	81.26	83	81	81.02	81	81		81.8	82.01	86				
900	82.99	82.99	82.36	83	81		82.05	81				86				
920	82.98	82.99	82.16	83	81			81				86				
940	82.99	82.99	82.99	84.29	82.19			82.6				86.98				

Figure 3.18: The timings of synchronous signal edges for four COPPERs at various reset delay settings through the previous firmware. The stable margin is about 5.4 ns from 2600 ps to 8000 ps.

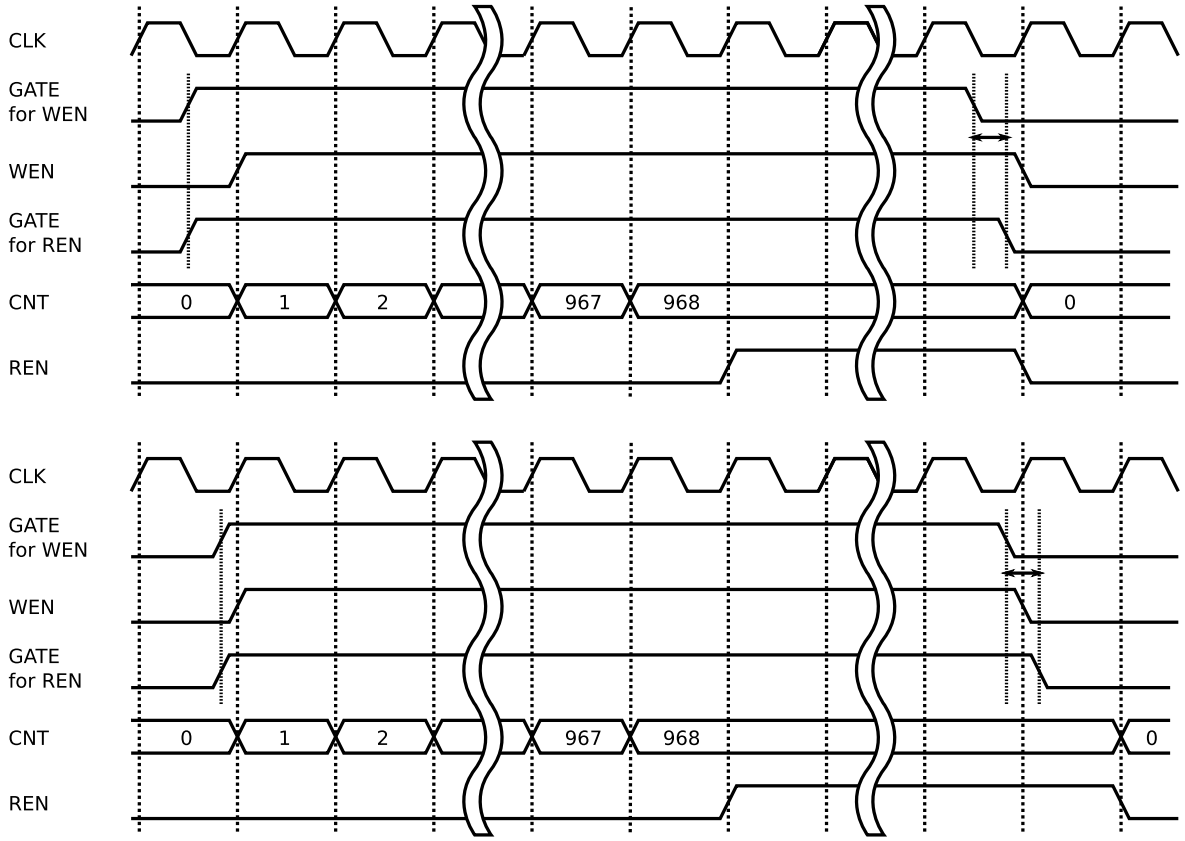

Figure 3.19: Timing chart of gate (GATE), write enable (WEN), and read enable (REN) signals latched by the same clock timing. GATE distributes the internal gate signals for WEN and for REN (GATEWEN and GATEREN). The timing that GATEWEN and GATEREN arrive at the modules can be different. FPGA sends WEN to FIFOs while the counter (CNT) stops sending REN to FIFOs.

3.3.2 Modification

The origin of the number of sample shifts seems to be the clock timing to make the WEN and REN by the gate. The gate signals was distributed to the modules to make WEN or REN as shown in Figure 3.20 (left). Figure 3.19 shows the timings of the WEN and REN separately latched. If the distributed gates in the FPGA have slightly different widths, the number of sample can be different because the subtraction of WEN and REN can be different. To resolve this issue, the gate should be latched in the FPGA at first, and then the latched gate should be distributed to the modules to make WEN or REN as shown in Figure 3.20 (right). The latch module in front of the two modules was installed by the firmware update.

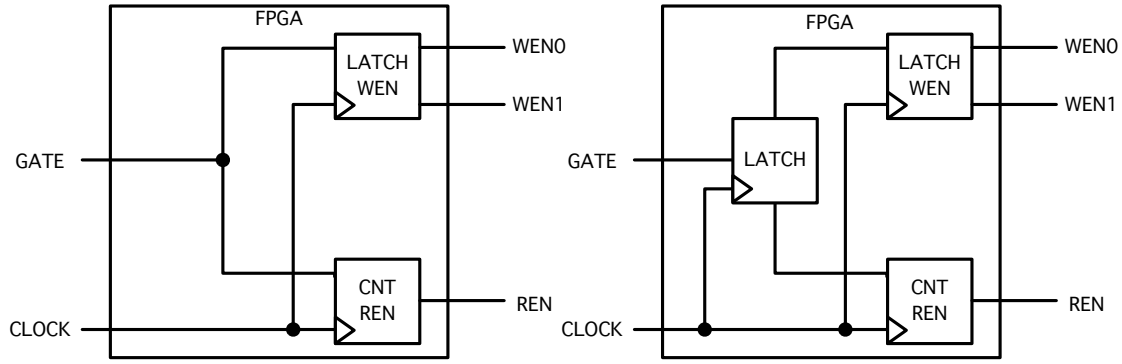

Figure 3.20: left: Diagram of a gate signal (GATE) distribution in FPGA. GATE is distributed to the modules to make write enable (WEN) and read enable signals (REN). right: Diagram of a latched gate signal (latched GATE) distribution in FPGA. The GATE is latched and then distributed to the modules to make write enable (WEN) and read enable signals (REN).

3.3.3 Result

The same test with the gate delay scan shows no shift of the number of sample with any delay timing for 1 Mevents. All of the numbers of sample table with the updated firmware have only 1936.

The modified firmware latches the gate in the beginning and send the branched latched gate for WEN, CNT and REN. The branched gate can have some difference but it is not so serious because they have enough margins although less than 8 ns. This firmware requires for the Clock Distributor variables to only adjust the timing of gate tailing edges to FINESSEs.

The changes of gate width can not also effect a number of samples. Figures 3.21 have a different timing of tailing edges but the number of samples are same. There is no shift in the number of sample ($< 10^{-7}$).

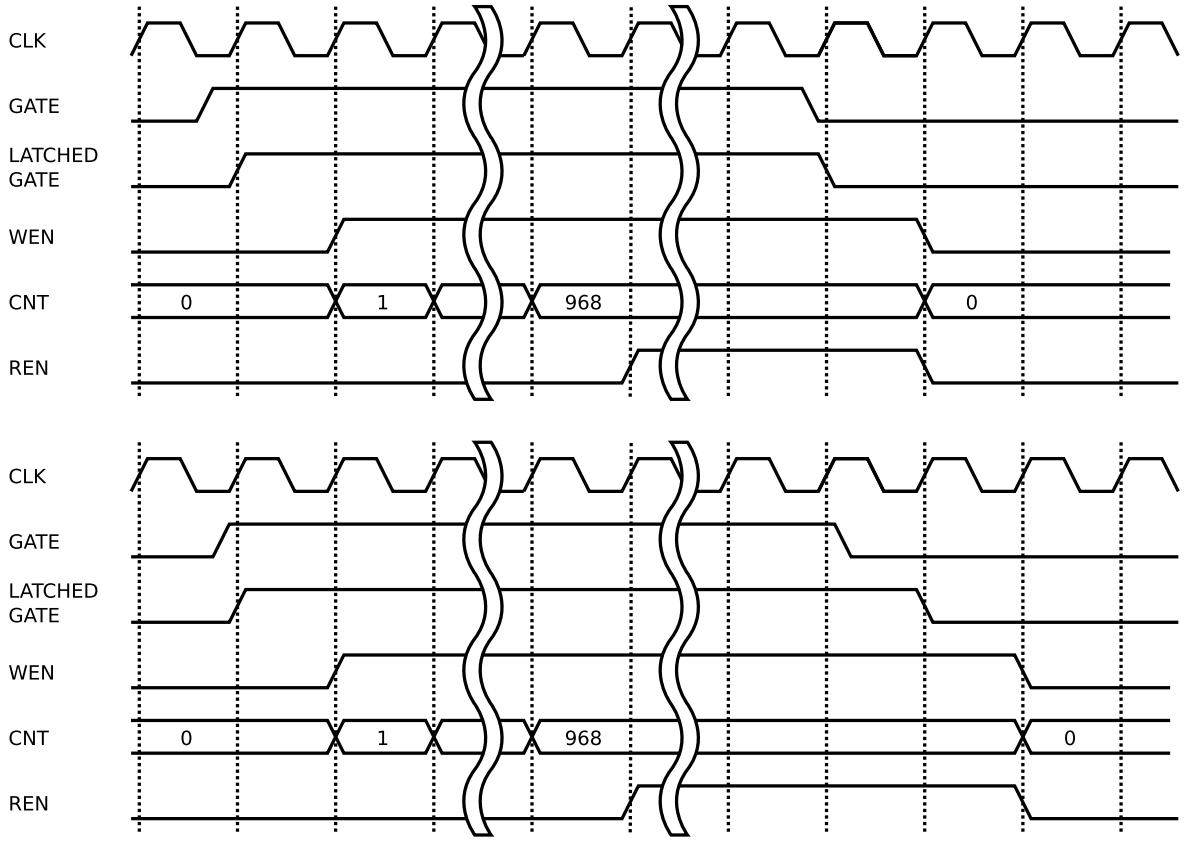

Figure 3.21: Timing chart of gate (GATE), write enable (WEN), and read enable (REN) with latched GATEs. The latched gate makes a WEN and the counter (CNT) which makes REN. The difference between WEN and REN lengthes is the data length.

3.4 Small Margin of Reset Timing

The purpose of the reset signal is to divide the 250 MHz clock to the 125 MHz clock. The Clock Distributor IC (CDIC) chip on FINESSE distributes the 250 MHz to four ADCs and the ADCs send the 125 MHz clocks to the FIFOs and the FPGA as shown in Figure 3.22. The 4 ns shift caused by the two phase 125 MHz is described in Paragraph 2.2.2

The COPPER board was not designed to acquire external reset signals. Therefore, there is no reset line from the trigger board to the FINESSEs. The contained line designed for other purpose was used for reset. The lines have different lengths which cause non-negligible timing differences. The different lengths caused the setup of CD to be difficult.

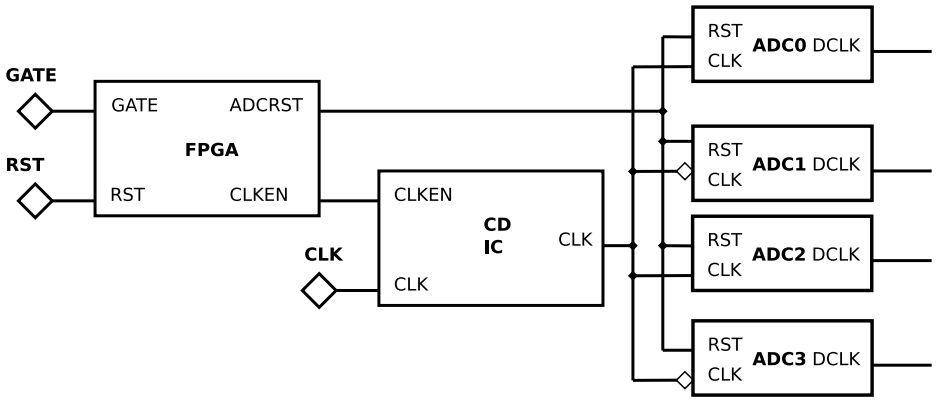

Figure 3.22: Diagram to reset the ADCs & Clocks.

3.4.1 Issue

The reset line length is different with each other because the COPPER system didn't expect the way to define the 125 MHz clock phase. When the reset signal is not synchronized with the CD 125 MHz clock for latching, 4 ns in each FIFOs can be different FINESSE by FINESSE.

Figure 3.23 shows the reset signal from the trigger board. The different line lengths cause the different timing to divide the 250 MHz clock to 125 MHz clock.

The addition of the extra input from FINESSEs is the simplest and reliable solution. However, it needs full replacement of more than 20 of FINESSE cards, and thus takes high costs.

The previous reset system causes the narrow margin of the stable value as shown in Figure 3.24 (left). The COPPER board received the reset from the trigger board on the end of COPPER. And the lines of reset signals to FINESSEs have different lengths as shown in Figure 3.23. Therefore, the suitable reset delays to FINESSEs were different with each other. Each FINESSEs has the enough margin which is 3.6 ns for the reset delay while the integrated suitable reset margin was 1.2 ns. The stability of the reset delay to the clock was worried in the long term.

3.4.2 Mdification

If the reset signal input to the FINESSE card with the same timing without adding any signal. that would solve the problem. A firmware update is one of the ideas to solve it.

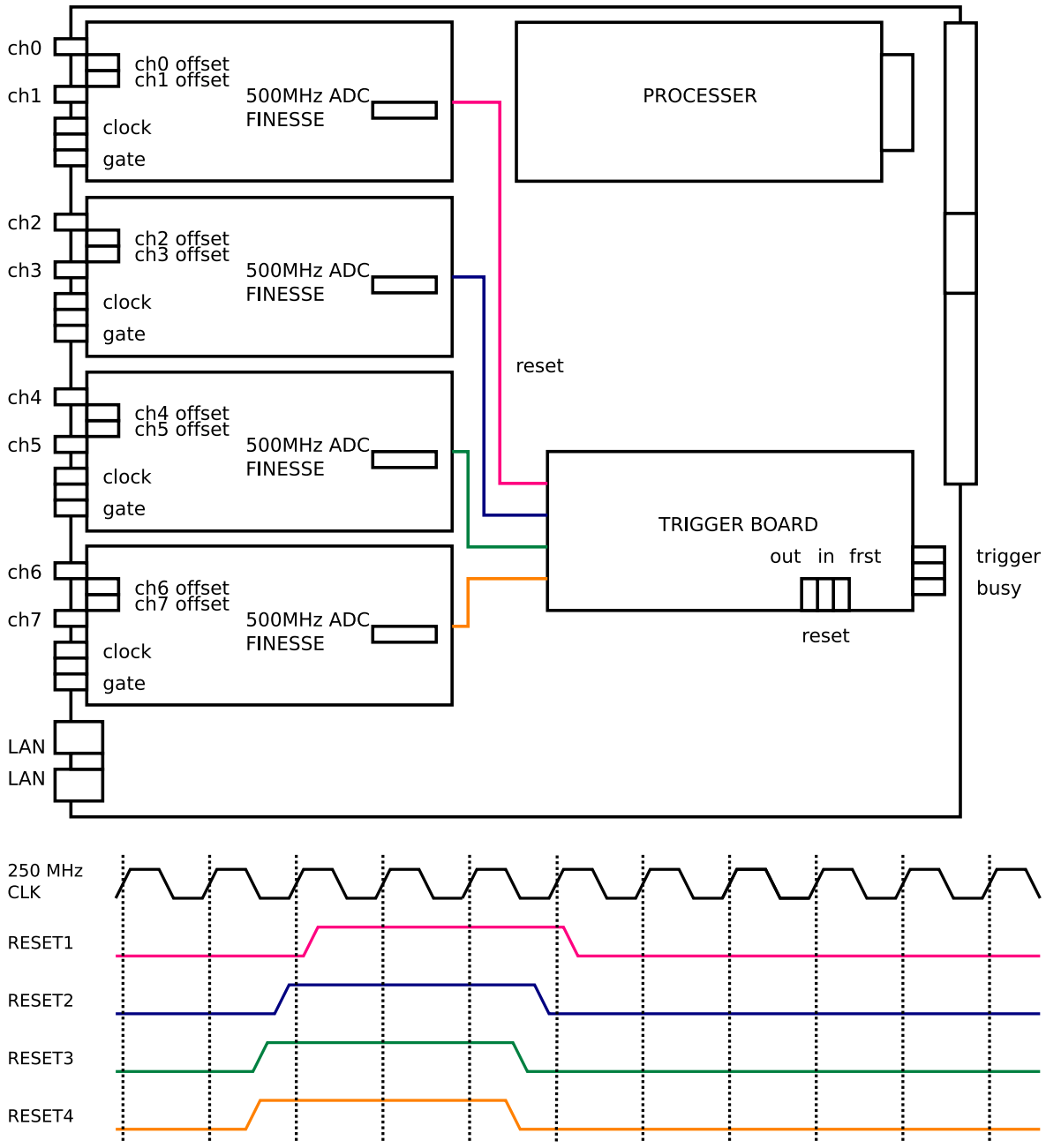

Figure 3.23: Schematics and diagram of the reset lines with different length. The different length allows the time of arrival at FINESSEs cross a clock timing.

Reset Delay (ps)	f1	f2	f3	f4
0	355	355	355	354
200	355	355	355	354
400	355	355	355	354
600	355	355	355	354
800	355	355	355	354
1000	355	355	355	354
1200	355	355	355	354
1400	355	355	355	x
1600	355	355	355	355
1800	355	355	355	355
2000	355	355	355	355
2200	355	355	355	355
2400	x	355	355	355
2600	354	355	355	355
2800	354	355	355	355
3000	354	x	355	355
3200	354	354	355	355
3400	354	354	355	355
3600	354	354	355	355
3800	354	354	x	355
4000	354	354	354	355
4200	354	354	354	355
4400	354	354	354	355
4600	354	354	354	355
4800	354	354	354	355
5000	354	354	354	355
5200	354	354	354	355
5400	354	354	354	354
5600	354	354	354	354
5800	354	354	354	354

Reset Delay (ps)	f1	f2	f3	f4
0	94	94	94	94
200	94	94	94	94
400	94	94	94	94
600	94	94	94	94
800	94	94	94	94
1000	93	93	94	94
1200	93	93	93	94
1400	93	93	93	93
1600	93	93	93	93
1800	93	93	93	93
2000	93	93	93	93
2200	93	93	93	93
2400	93	93	93	93
2600	93	93	93	93
2800	93	93	93	93
3000	93	93	93	93
3200	93	93	93	93
3400	93	93	93	93
3600	93	93	93	93
3800	93	93	93	93
4000	93	93	93	93
4200	93	93	93	93
4400	93	93	93	93
4600	93	93	93	93
4800	94	94	93	93
5000	94	94	94	93
5200	94	94	94	93
5400	94	94	94	94
5600	94	94	94	94
5800	94	94	94	94

Figure 3.24: Left: The timings of synchronous signal edges at various reset delay settings through a previous firmware. The different line length of reset signal allows each FINESSEs to have each stable values. The stable margin to all FINESSEs is about 1.2 ns from 4000 ps to 5200 ps without concerning the value. The other stable margin to every FINESSEs is about 0.6 ns from 1600 ps to 2200 ps with concering the value. Right: The timings of synchronous signal edges at various reset delay settings through the previous and modified firmware. The stable margin to every FINESSEs is about 3.2 ns from 1400 ps to 4600 ps.

Reset Signal from FINESSE cards

The original reset input was changed to the reset enable (RSTEN) signal. Furthermore, the gate input was changed to the reset or gate input. Figure 3.25 shows the way to select the signals from the same input. The new reset signal come from the gate or reset input when RSTEN is on while the gate signal come from the gate or reset input when RSTEN is off. This method doesn't need any hardware modification to add inputs on FINESSE or modification of COPPER boards.

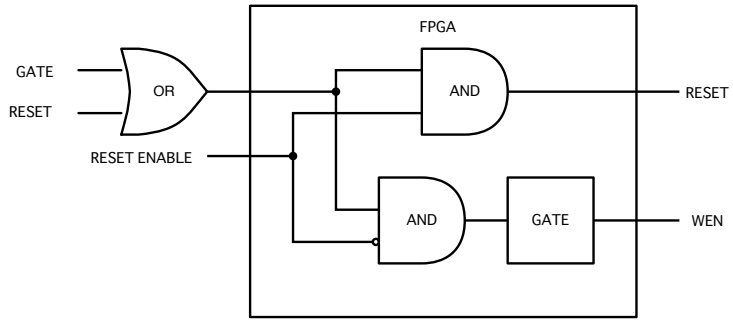

Figure 3.25: Diagram of select gate or reset from FINESSE input. Reset signals initialize the internal 125 MHz clocks, and gate signals make write enable signals to FIFO. Reset enable signal select gate or reset by logical AND in FPGA.

Reset Enable by GPIO Update

The updated reset scheme requires the reset enable signal. The reset enable signal was created by GPIO updates. GPIO had created the reset signal (RST_OUT) by the reset signal from VME (RST_IN). GPIO can create the reset enable signal (RSTEN_OUT) by the firmware update. Figure 3.26 shows the scheme to create the reset and reset enable signal. COPPER sends a busy signal to GPIO (CPRBSY_IN) after it receives the reset signal from GPIO.

3.4.3 Results

The new system has wider range of the suitable reset delays (3.2 ns) as shown in Figure 3.27 better than the previous one (1.2 ns) as shown in Figure 3.23. Each margins of FINESSEs didn't change but the combined margin is totally different with the previous one. The new firmware on FINESSE allows each FINESSE to receive the reset signal from the input of each FINESSEs. Therefore, every ADC on FINESSEs are reset by the same timing.

Figure 3.24 (right) shows the stable reset delay for the 4 COPPERs used in PIENU. The margin is 2.8 ns enough to be stable for long time operation.

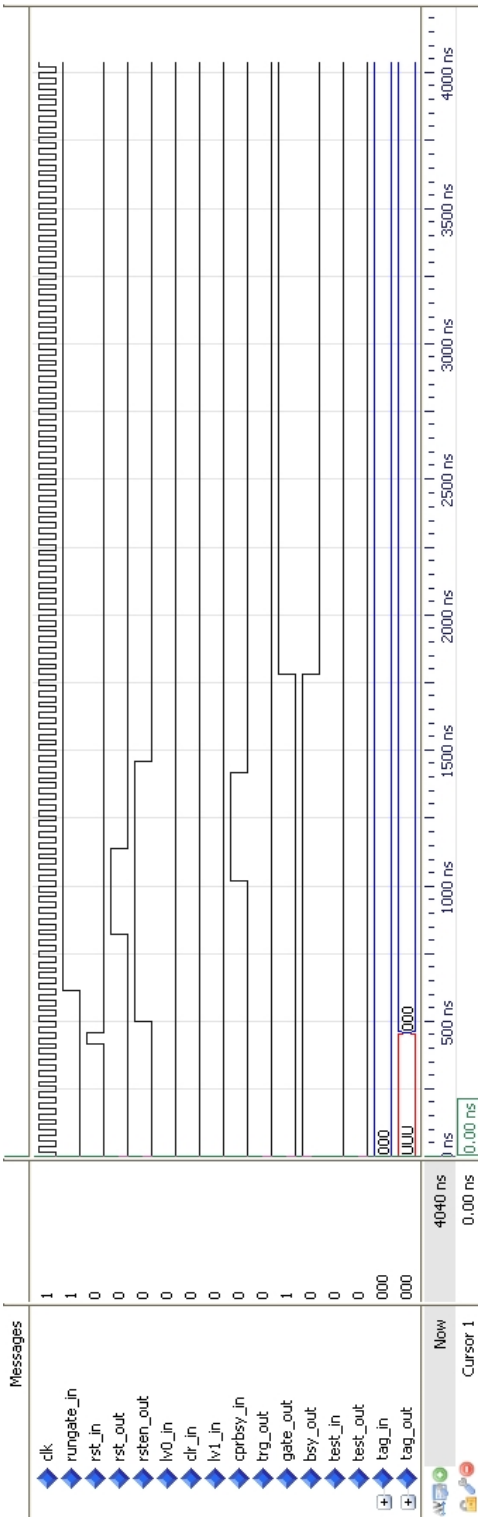

Figure 3.26: Reset enable signal. The reset signal from VME (RST_IN) creates the reset signal for COPPER (RST_OUT) and the reset enable signal (RSTEN_OUT). An internal veto signal exists for 300 ns after the RSTEN_IN closing. The other signals are for the trigger logic described after.

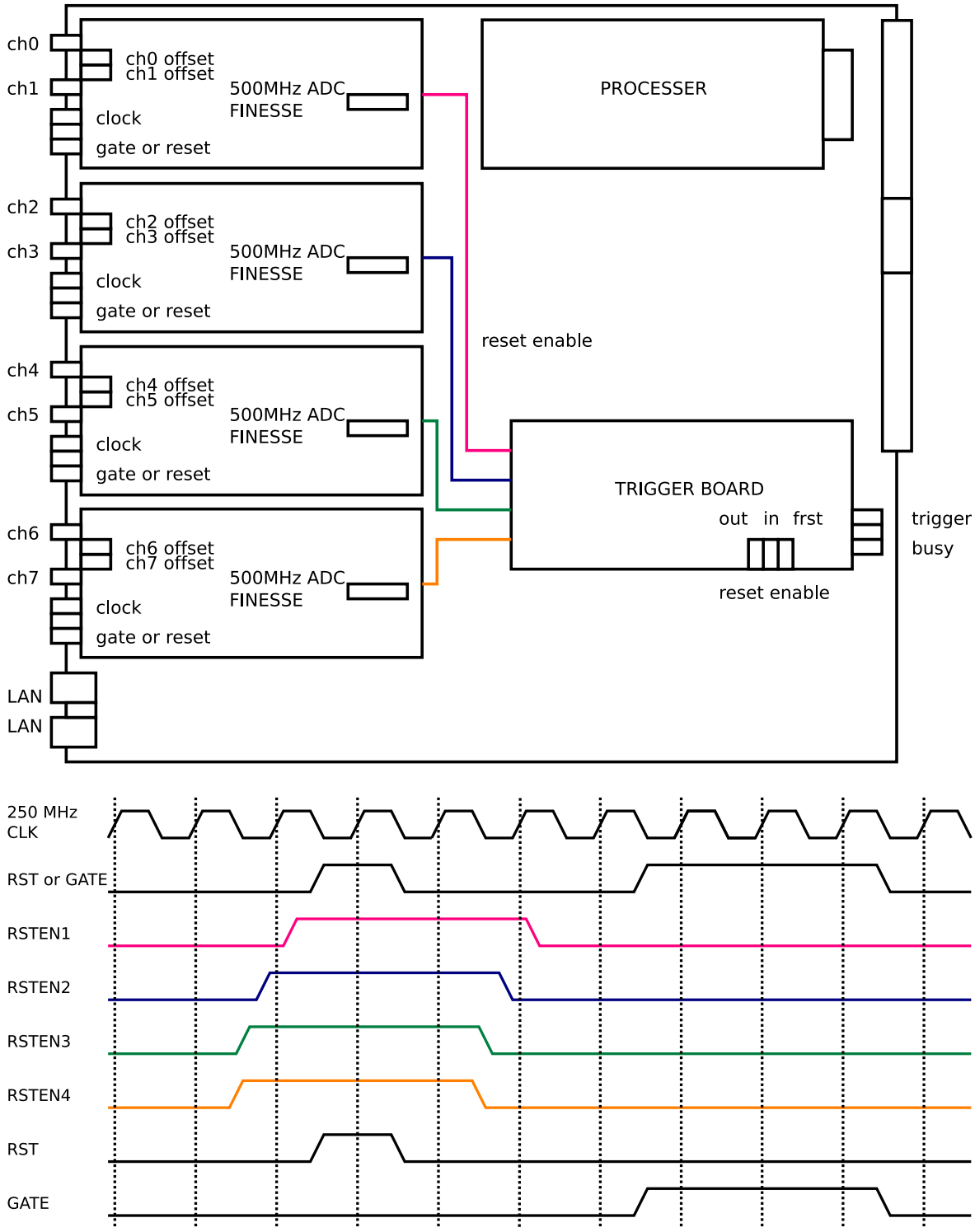

Figure 3.27: Timing chart of the reset from gate input AND the reset enable from the trigger card

Signal Edge Timing	c1				c2				c3				c4			
Reset Delay	f1	f2	f3	f4	f1	f2	f3	f4	f1	f2	f3	f4	f1	f2	f3	f4
40													94	93	94	92
60													94	93	93	92
80	94	94	94	94	94	94	94	92	94	94	94	97	93	93	93	92
100	93	93	94	94	94	93	94	92	93	93	94	97	93	93	93	91
120	93	93	93	94	93	93	93	91	93	93	93	96	93	93	93	91
140	93	93	93	93												
160	93	93	93	93												
400																
420													93	93	93	91
440					93	93	93	91					93	94	94	91
460	93	93	93	93	93	93	93	91	93	93	93	96	94	94	94	92
480	94	94	93	93	93	94	93	91	93	94	93	96				
500	94	94	94	93	93	94	93	91	94	94	93	96				
520	94	94	94	93	94	94	94	92	94	94	93	96				
540	94	94	94	94					94	94	94	97				

Figure 3.28: The timings of synchronous signal edges for four COPPERs at various reset delay settings through a modified firmware The stable margin is about 2.8 ns from 1400 ps to 4200 ps.

3.5 Summary

The modifications of the firmware on FINESSE 500-MHz FADC resolved the three issues related to the reliability of the COPPER system. The clock timing adjusted by the firmware eliminate the ADC timing shift errors and enhanced the data reliability. The ADC timing shifts didn't happen ($< 10^{-9}$) at the Autumn run in 2009 after the modification although the ADC timing shift happened with the frequency of 10^{-7} - 10^{-2} at the Summer run in 2009 before the modification. The number of sample points shifts had been also disappeared ($< 10^{-7}$) by the distributing the latched gate to the modules for WEN and REN in the FPGA. At last, the reset timing margin became more wider ~ 3.2 ns from ~ 1.2 ns, and allowed the stability enhanced.

Chapter 4

Upgrades of COPPER 500-MHz FADC System

4.1 Motivations of COPPER 500-MHz FADC System Upgrade

The new DAQ and trigger system are being installed to enhance the quality and quantity of the data. In order to achieve the installations, the COPPER FADC system have to be also modified. The firmware update adapted the COPPER system to the requirements to install. The following two functions are installed by the firmware on GPIO and FINESSE:

- Two level trigger for digital sum trigger,
- Time stamp for new event building system.

The digital sum trigger module required the two level trigger for COPPER to restore the 2 μs of time window which could be lost by trigger decision time of the new trigger scheme. data gone away by the decision time of the new module. The firmware on GPIO was updated for the two level trigger. The time stamp was installed on FINESSE for the new event building system which is required by the updated read-out system of other modules.

This chapter describes the upgrades of the new systems and the adaptations of FINESSE and GPIO by firmware

4.2 Level 0+1 Trigger by GPIO Firmware Upgrade

A digital sum trigger of calorimeter in place of the analog sum trigger is required for good energy selections. The module to integrate the digital sample and to decide the threshold takes 2 μs for the decision. The 2 μs data should be monitored by 500-MHz FADCs for the information of old muon. The old muon can decay after the pion trigger to the positrons which cause backgrounds in the positron spectra. In order to secure the 2 μs caused by the trigger decision time, the level 0+1 trigger was installed by the firmware of the GPIO module.

4.2.1 Digital Sum Trigger Module Installation

The digital sum trigger of the NaI and CsI signals is created by the TIGC module. The TIGC module was developed by TRIUMF and closely connected with the VF48 60 MHz FADC developed by

TRIUMF. It integrates the digital signals and decides the trigger by a digital threshold.

The BinaHigh and CsIHit triggers had taken the high energy positron data for $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ decay. The analog sum trigger decided by the NIM modules allows the trigger rates without $\pi^+ \rightarrow e^+ + \bar{\nu}_e$ data to be enhance because the analog sum trigger has the loose threshold to take the data withou bias. The analog sum had about one hundred signals and the bad resolution from attenuations.

The PIENU experiment is using the VF48 module for NaI and CsI signals. Therefore, the digital inputs to the TIGC module had already existed.

The VF48 60 MHz FADC with a maximum rate of 60 Msps is used for the calorimeters. TIGC can make the integration and decision with the digital data from VF48. And it also can make the trigger by the better energy resolution without attenuations.

The digital sum trigger takes about 2 μs for the decision time, so the time window of the COPPER will be shifted as shown in Figure 4.1. The time window shift wastes the old muons which was visible for 2 μs. The muons cause the background in the positron time spectrum because the muon can stop in the target and emit the positron with the lifetime 2.2 μs after trigger pion. The muon should be monitored for the 2 μs.

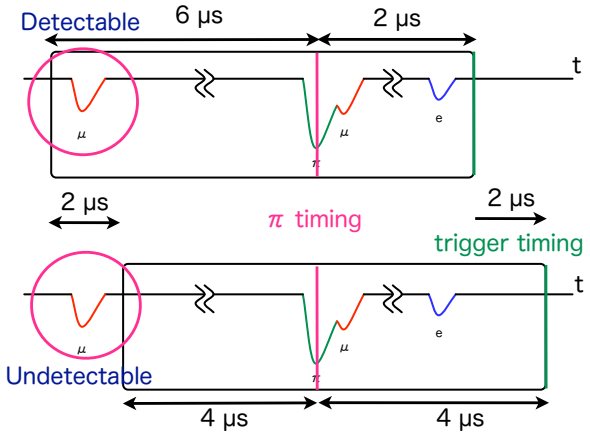

Figure 4.1: Schematic diagram of the trigger delay by TIGC.

4.2.2 Level 0+1 Trigger by GPIO Firmware Update

Level 0+1 trigger to save the 2 μs data was installed by GPIO firmware update. The GPIO module creates the signals for the interface between COPPER and the upstream trigger logic. Therefore, the modification of GPIO could solve the digital sum problem.

Level 1 (LV1) trigger is made by the TIGC module and takes 2 μs for trigger decision while Level 0 (LV0) trigger is made by the B counters $\cap$ Tg counter $\cap$ T counters and has same timing with the previous trigger. LV0 trigger keeps the buffered data and LV1 trigger transfer the data from FINESSE to the COPPER board. If the LV1 doesn't come after LV0, the data is cleared by the automatic reset. The automatic reset is installed on GPIO by a counting module. The only LV1 trigger also allows the logic to take the data which the previous trigger logic.

Figures 4.2 show the previous and updated COPPER trigger logic for PIENU. The previous trigger consisted of four triggers. The updated trigger has the slow decision TIGC trigger in place of the

analog triggers of NaI and CsI. With the updated trigger logic, the coincidence module can create the LV0 trigger because it is almost same with the previous trigger timing. And then, the LV1 trigger after the TIGC decides the data transfer timing

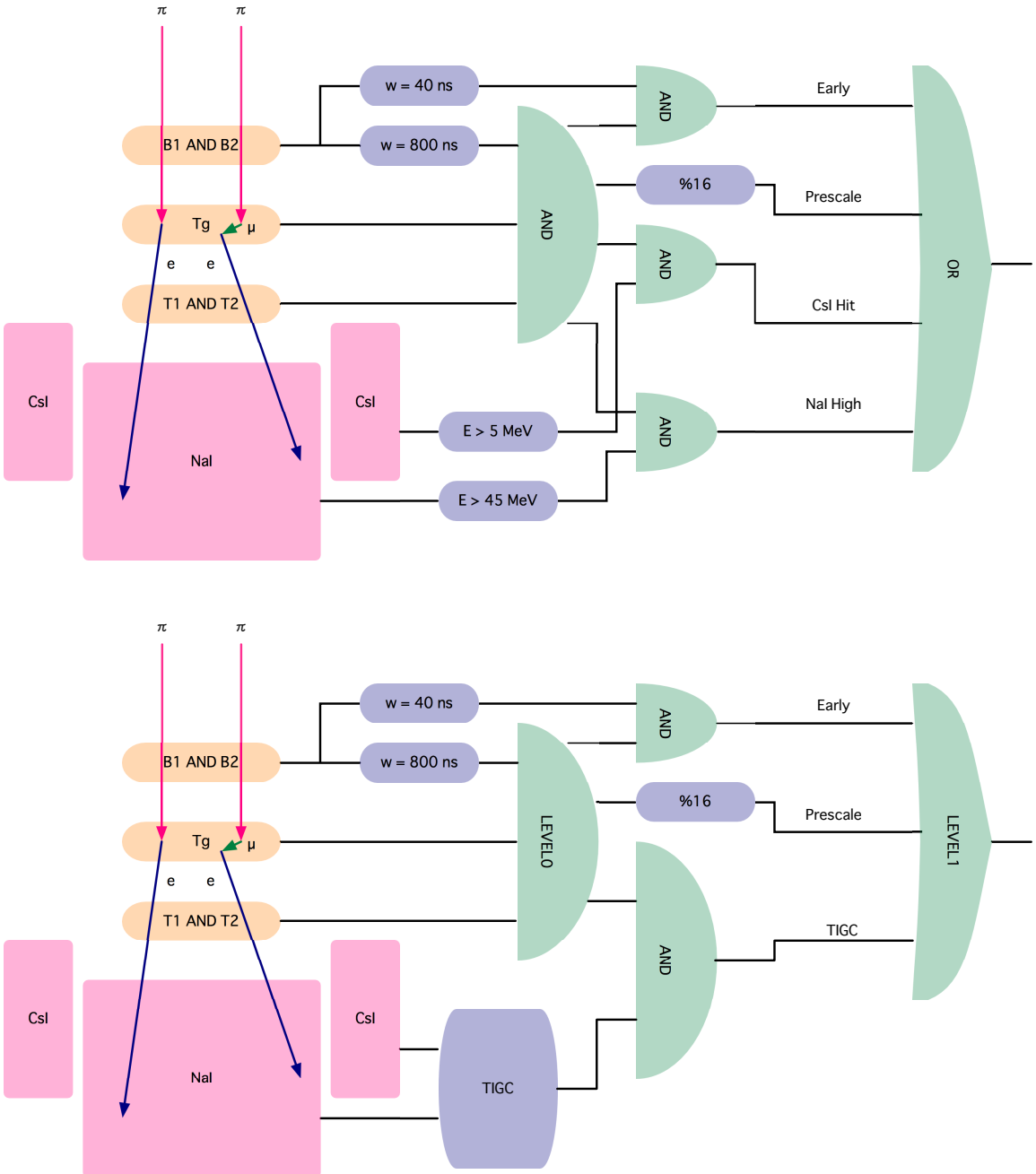

Figure 4.2: PIENU trigger diagram upgrade.

GPIO controls COPPER to buffer waveforms during the gate signal is on transfer the data from FINESSE to COPPER by the trigger signal. Therefore, the gate close timing should be LV0 and trigger should be LV1. Figures 4.3 shows the connections between COPPER modules with the previous and updated GPIO. The GPIO with the updated firmware has LV0 and LV1 inputs from the upstream NIM logic. And the reset enable signal is for the new reset logic described in section 3.4.

The previous trigger stopped the gate and send the COPPER trigger after about 300 ns to transfer the data from FINESSE FIFOs to the COPPER board as shown in Figure 4.4. And then, the end of the busy signal from COPPER opens the gate again.

The updated GPIO closes the gates by the LV0 and creates the COPPER trigger by the sequent LV1 trigger in Figure 4.5. The LV1 trigger without LV0 can happen by other calibration triggers. The only LV1 trigger allows GPIO to send the signals like the previous logic. When LV1 doesn't come after LV0, GPIO waits for about 2.5 μs and then open the gate again as shown in Figure 4.6. The new gate can take the new data because the FINESSEs' firmware resets the FIFOs when they receive new gates. These timing charts were created by the simulation software, ModelSim [5].

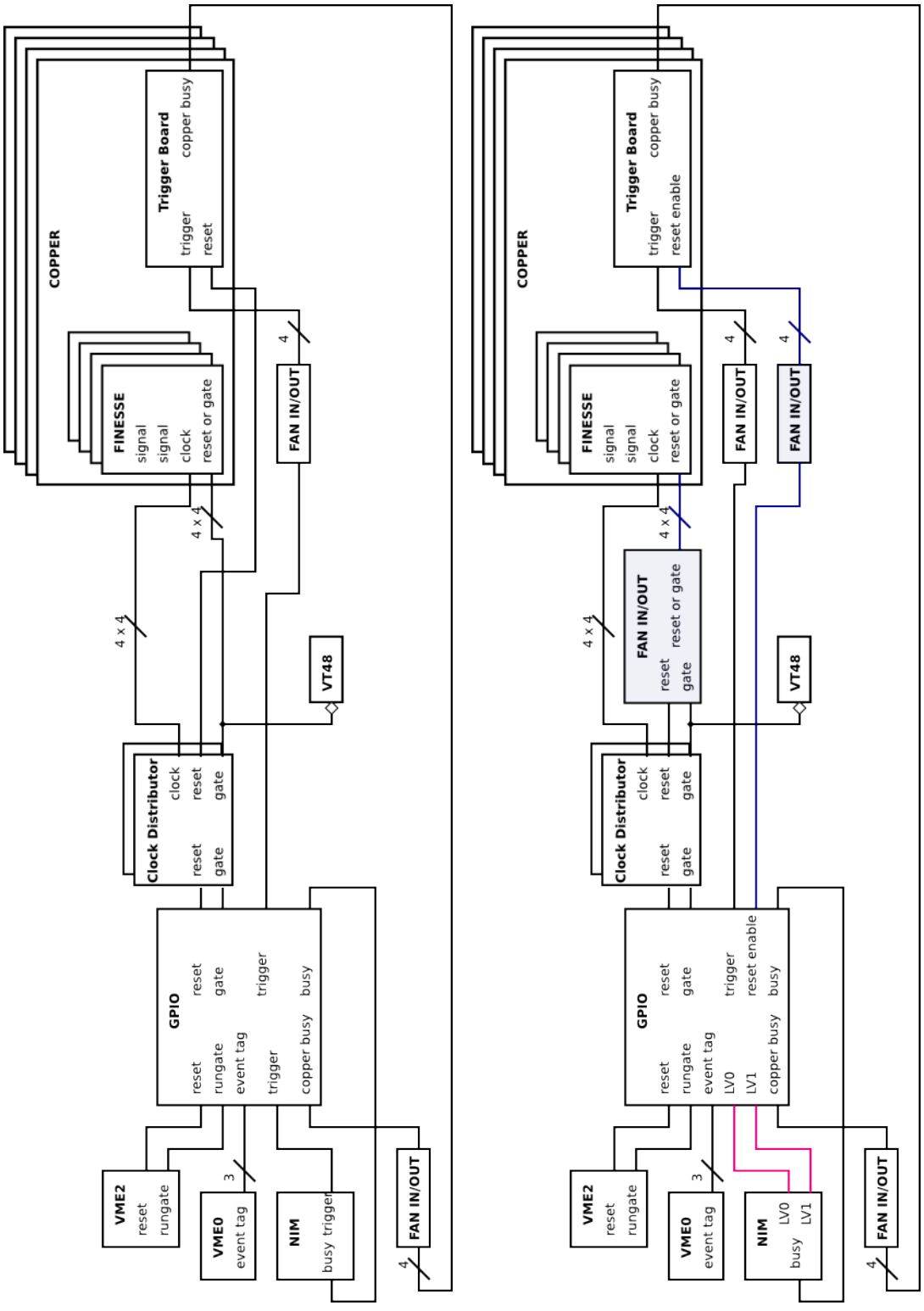

Figure 4.3: Logic diagram upgrade for COPPER in PIENU. Left: The upstream trigger creates the COPPER trigger and gate signals. The reset signal from VME goes to COPPER reset through GPIO. Right: The upstream LV0 trigger stops the gate signals and the LV1 trigger creates the COPPER trigger. The reset signal from VME goes to FINESSE input through GPIO and FAN IN/OUT to merge with gate signal. The reset enable created by GPIO goes to a trigger board.

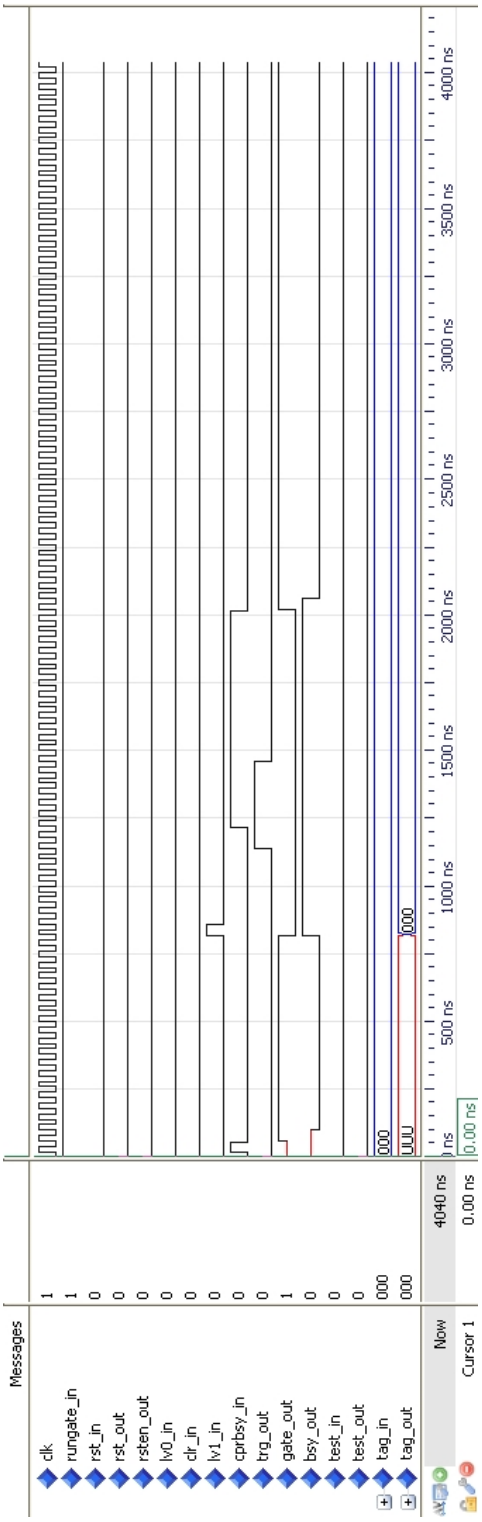

Figure 4.4: Level 1 trigger. This trigger is same with the previous one. level 1 trigger (LV1_IN) stops the gate (GATE_OUT) and starts the busy (BSY_OUT), and sends the trigger for COPPER (TRG_OUT) after a few hundred ns. And then the closing timing of busy (CPRBSY_IN) starts GATE_OUT and stops BSY_OUT, respectively.

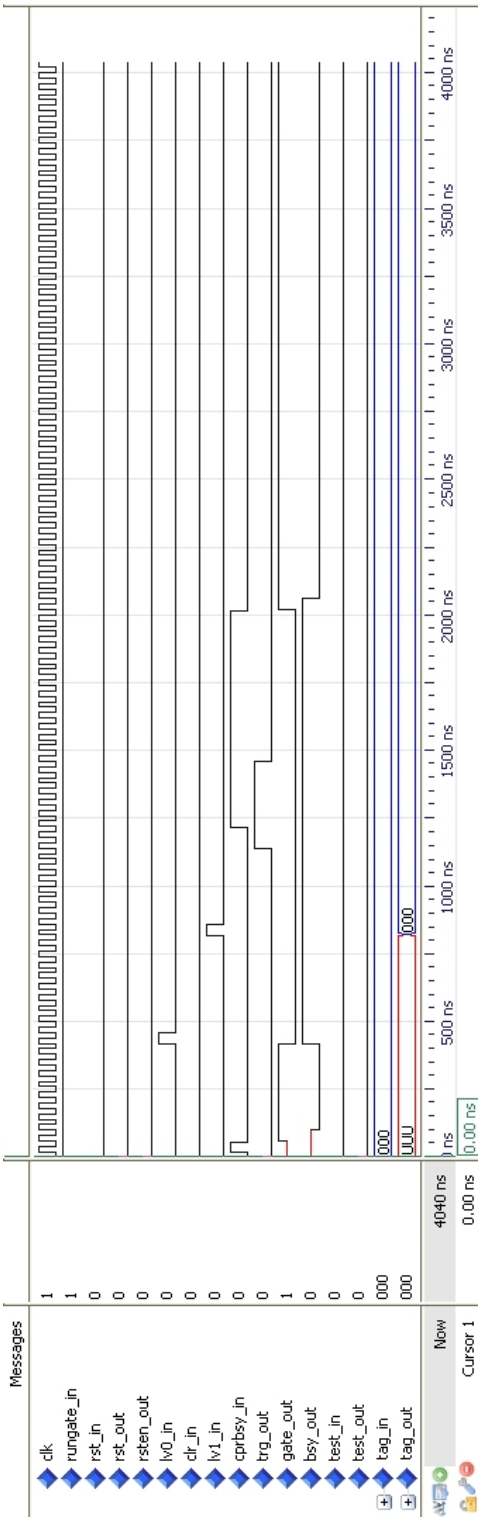

Figure 4.5: Level 0 + 1 trigger. level 0 trigger (LV0_IN) stops the gate (GATE_OUT) and starts the busy (BSY_OUT), and level 1 trigger (LV1_IN) sends the trigger for COPPER (TRG_OUT) after a few hundred ns. And then the closing timing of busy (CPRBSY_IN) starts GATE_OUT and stops BSY_OUT, respectively.

4.2.3 Tests of Level 0+1 Trigger

The data with only LV1, with LV0 and LV1, and with only LV0 trigger are checked by the test bench and the PIENU trigger logic. The function of GPIO and the time window of COPPER is investigated.

Figure 4.7 show the waveforms of the calorimeter without and with the level 0 trigger. The positron beam hit the NaI calorimeter through B1 and T1 scintillators. The level0 trigger apparently saves the region before the trigger.

The only LV0 trigger was checked to automatically clear the gate and restart to take the data without hanging.

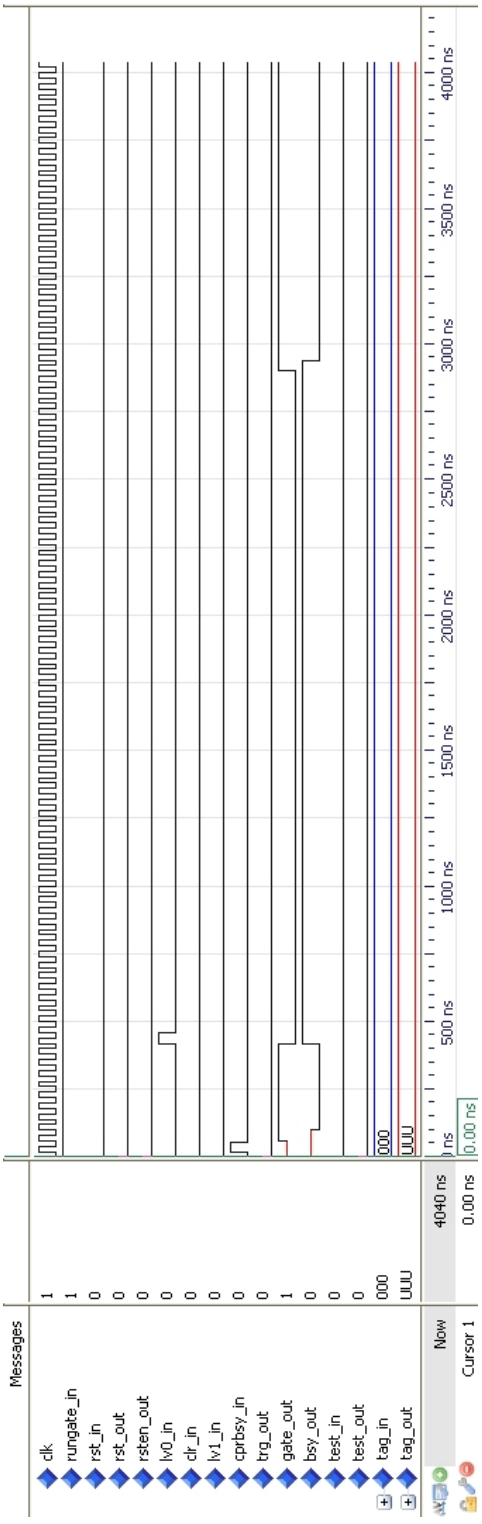

Figure 4.6: Auto clear. No level1 (LV1) and no clear signal (CLR_IN) after a level 0 trigger creates the auto clear by CLEARCOUNTER to reset the gate (GATE_OUT) and the busy (BSY_OUT).

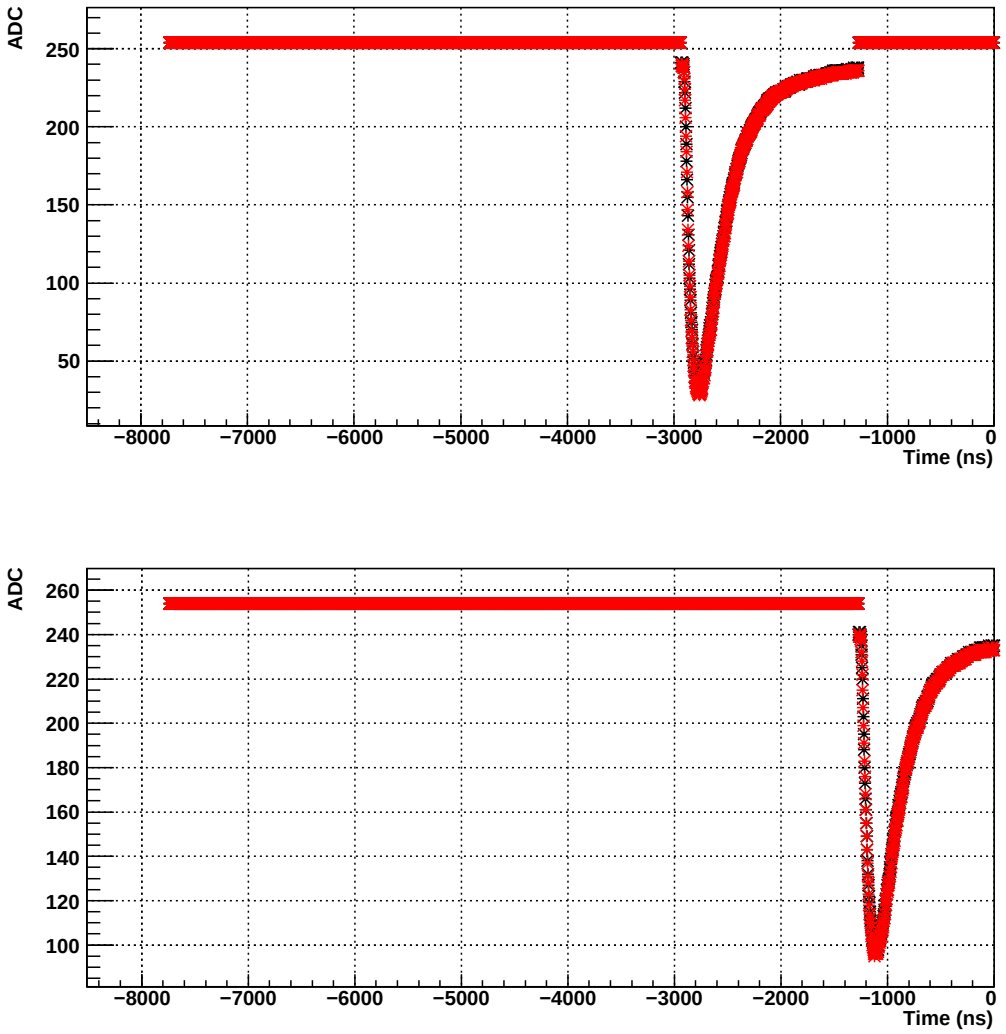

Figure 4.7: Waveforms of 1st COPPER with level 1 trigger, with level 0 + 1 trigger.

4.3 Time Stamp FINESSE 500-MHz FADC Firmware Upgrade

The time stamp function was installed on the firmware of the FINESSE 500-MHz FADC because the upgraded read-out system requires the event building system based on the time stamp. This section shows the requirement and installation of the time stamp.

4.3.1 Read-out System Update

The PIENU experiment is using not only COPPER 500-MHz FADC but also the VF48 60-MHz FADC and VT48 TDC developed by TRIUMF. The data of all modules should be merged trigger by trigger. However, VF48 and VT48 have larger dead-time than COPPERs to transfer data trigger by trigger. Therefore, the read-out system is planed to be updated.

The PIENU experiment takes the data by VF48, VT48, COPPER, and slow control modules. Figure 4.8 shows the hardware configuration of the DAQ. The DAQ Network consists of two VME crates controlled each by a VMIC CPU, four COPPER CPUs, one high performance computer PIENU01 as the host computer, one CAEN HV mainframe, one computer PIENUSC connected to slow control devices. All components are interconnected through GigaBit Ethernet switch. The PIENU01 computer has a second Ethernet controller connected to the second network switch which is a part of the site network. PIENU02 is a high performance machine dedicated to online reconstructing and monitoring. M13BEAM is the computer used mainly to access the M13 beam line control system.

The PIENU experiment uses Maximum Integration Data Acquisition System (MIDAS) for data taking and constructing. PIENU01 is the MIDAS main server which controls each front-end on all processors. Main informations can be monitored through the PIENU MIDAS web pages.

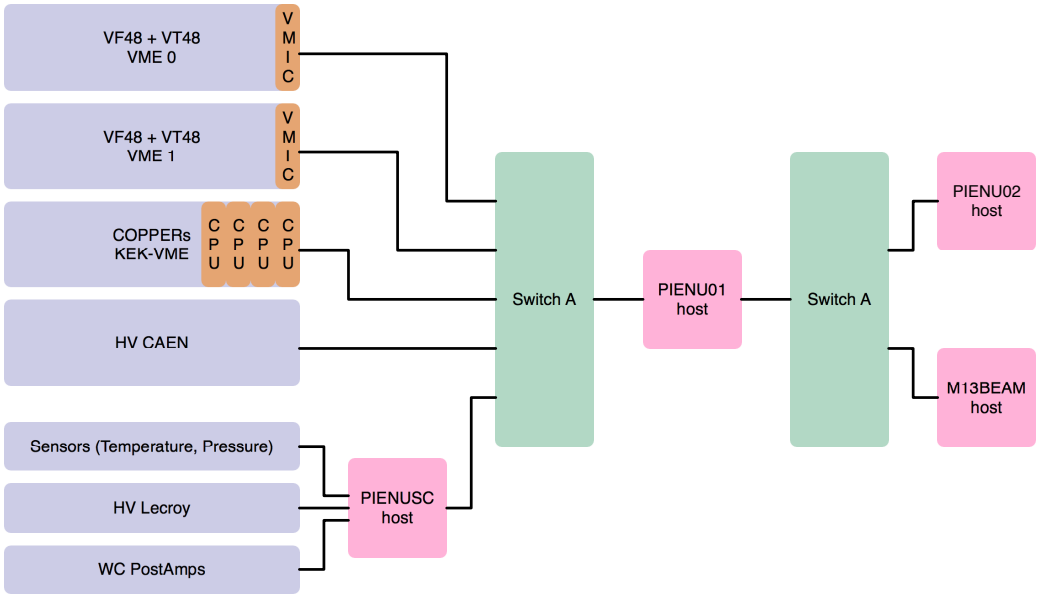

Figure 4.8: Schematics of DAQ network.

Table 4.1 is the readout time and live time of VME0 and VME1. COPPERs don't effect the dead times because COPPERs have the on-board PC front-ends. VF48s followed by VT48s limit the DAQ

rate for now. The statistics can affect the branching ratio precision. Therefore, the readout system is required to be updated.

Table 4.1: VME readout time & live time.

Modules	VME0 (μs)	VME1 (μs)	Rate (Hz)	Live Time (%)
COPPER + VF48s + VT48s	360	335	560	69%
COPPER	17	18	660	83%
COPPER + VF48(VME0)	336	18	560	69%
COPPER + VF48(VME1)	17	340	575	66%
COPPER + VT48s	117	18	650	80%

The DAQ update of VF48 and VT48 is being planned because VF48 and VT48 dead-time limits the trigger rate. The data of VF48 and VT48 start to be taken by a trigger timing for now. The update expects to decrease the sending time by asynchronous data taking because the dead-time mainly comes from the time sending the data via VME bus.

The subsequent program is the event building system. The current DAQ build the events trigger by trigger on PIENU01. New DAQ cannot build events trigger by trigger because of the asynchronous data taking. Two informations is considered to identify the data. One is event numbers, and the other is time stamp. The FINESSE 500-MHz FADC has only event numbers. Therefore, the COPPER 500-MHz FADC was required to have time stamp by a firmware update.

4.3.2 Time Stamp by FINESSE Firmware Update

The 64-bit time stamp operated with the 62.5 MHz counter divided from FPGA 125 MHz clock is installed in the FPGAs on FINESSE. This feature is enough for the PIENU experiment because the trigger rate is about 1 kHz and 1 run is less than two hours. 64-bit time stamp can count about 8,000 years, but 32-bit time stamp counts only 124 sec. One of the reasons to use 62.5 MHz clock is that 125 MHz exceeds the capability of FPGA clock line.

The time stamp value is the counter value when the trigger comes. A memory reads the counter number when the gate signal is open. The memmory keeps the last value of the counter when the gate signal is closed as shown in Figure 4.9. This means the timestamp is the counter number at the level0 trigger timing.

The front-end and analysis programs were also modified because the data structure was changed.

4.3.3 Tests of Time Stamp

Figure 4.10 shows the time stamp versus the event number on one FINESSE. The pulser trigger makes the time stamp be exactly proportional to the event number. The rate of pulser and the gradient of timestamp to event number are consistent. The following test was also performed with a pulser trigger.

The events followed by the previous event should come with almost same intervals. The difference of two timestamps between an event and the next event was investigated. Since the trigger is made by pulser for this test, the subtraction had the Gaussian distribution as shown in Figure 4.11.

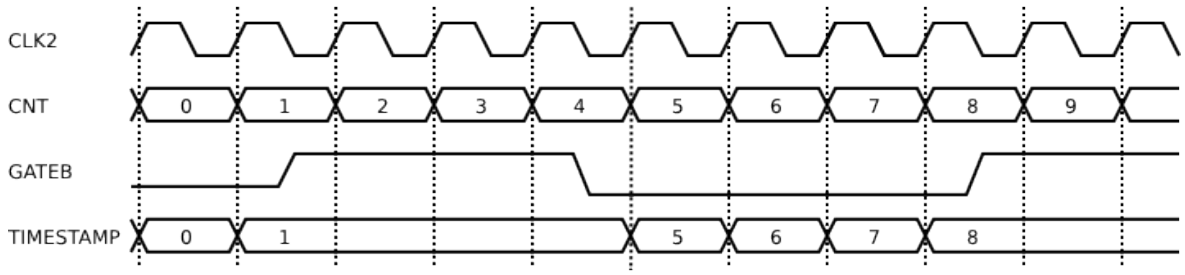

Figure 4.9: Timing chart of the time stamp. The time stamp (TIMESTAMP) buffers the number of counter at the gate (GATEB) closing.

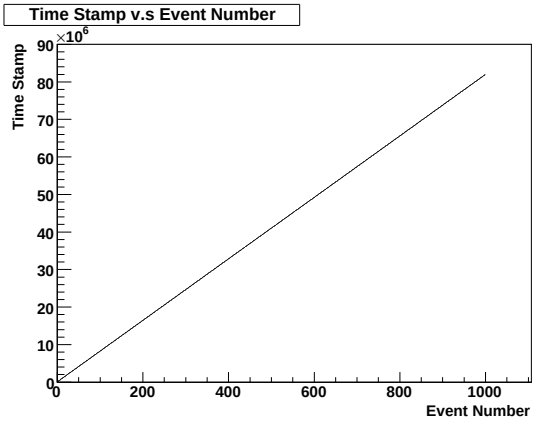

Figure 4.10: Time stamp versus event number. The pulser trigger made the time stamp be proportional to the event number.

The four FINESSEs cards on a COPPER should be synchronized. I checked the timestamps all of them. Figure 4.12 shows the difference between FINESSEs. The value was the same for 1 Mevents with asynchronous pulser triggers.

The carried digit failure was also suspected when many digits shift at the same time. For example, the trigger at the counter number changing from 0xffff ffff ffff to 0x1 0000 0000 0000 or from 0x7fff ffff ffff ffff to 0x8000 0000 0000 0000 looks very delicate. However the number is very stable for 100 kevents in Figure 4.13. This test is operated by adjusting the initial number of time stamp.

The time stamp is sufficiently stable for PIENU experiment. The stability must come from the simplicity of the firmware design because the extra flags for changing statements caused unstable state at the first design.

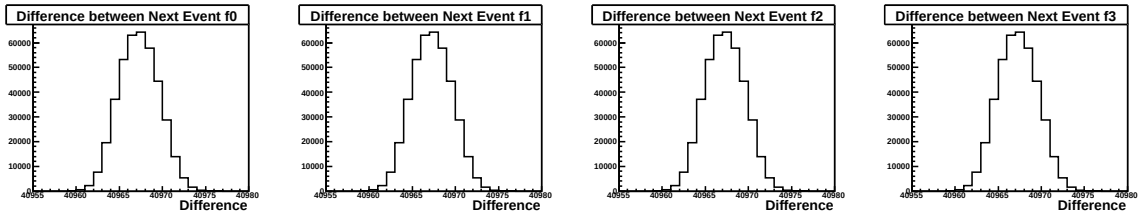

Figure 4.11: Difference of timestamps between an event and the next event. No large jump is detected by a pulse generator.

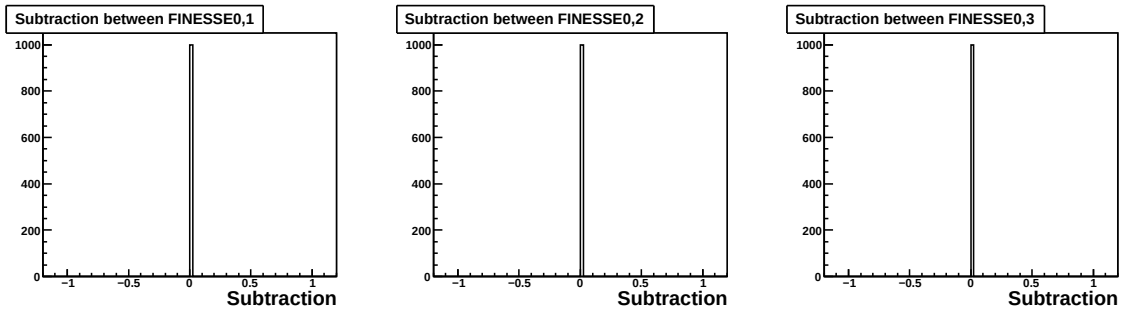

Figure 4.12: Difference of timestamps between four FINESSEs. No difference is detected.

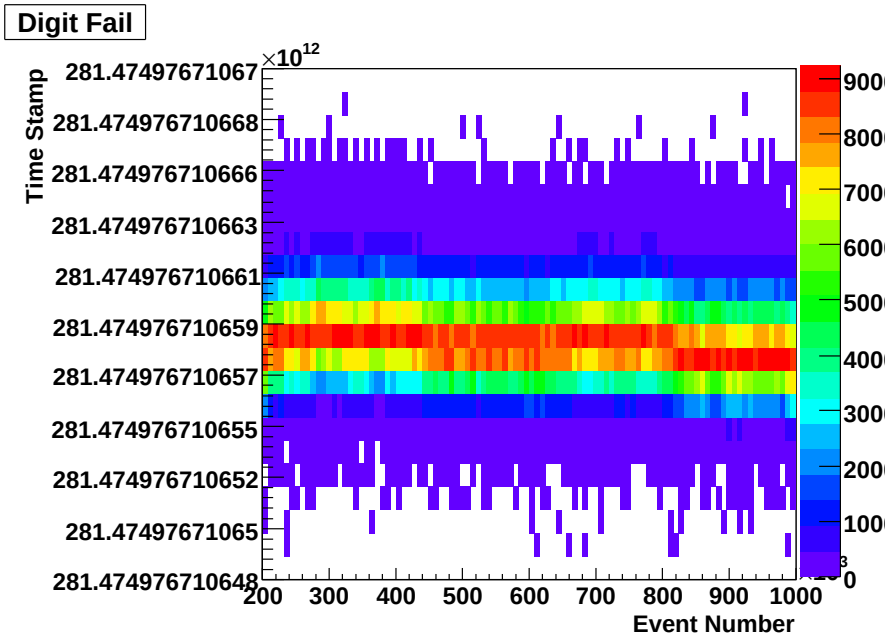

Figure 4.13: Event ID versus Timestamp. The timestamps at carrying the digit is studied. The triggers after each resets caused the almost same timestamp. 281474976710655 is 0x ffff ffff ffff. 281474976710656 is 0x 1 0000 0000 0000. In the out of Y axis, there are no event.

4.4 Summary

The two requirements to COPPER for the new system were achieved by the firmware updates. The GPIO provided the two level trigger mode by the firmware update. It saved the 2 μs data reduced by the installation of the digital sum trigger for calorimeter signals. And the other triggers without update can take data with no change because GPIO kept up with simple trigger. The visible old muons by the trigger update can decrease the backgrounds in the positron time spectrum.

The time stamp function was installed by the firmware update of the FINESSE 500-MHz FADC. This upgrade allows the new event building system between COPPER and VF48, VT48. The COPPER system is ready to build events by the time stamp for the installation of the new read-out DAQ system.

One of the concepts to develop the COPPER system was ease of developments and updates. The concepts was proved by these adaptations of the COPPER system to the DAQ updates

Chapter 5

Summary

The PIENU experiment to measure the pion branching ratio by less than 0.1% precision begun to take physics data from April 2009. The COPPER 500-MHz FADC exceedingly contributes to decrease the systematic errors in the experiment. The updates of COPPER modules' firmwares solved three issues and allow two adaptations to other DAQ updates.

The ADC timing shift disappeared by the firmware update on FINESSE. The gate signal controlled by the 125 MHz was adjusted by 90 degrees. 10 Mevent data on test bench with the synchronous signals have no shift of the data. Furthermore, the rate of the endcode error which shows the last data missing in FIFOs became $< 10^{-9}$ from 10^{-7} - 10^{-2}. The endcode error had a temperature dependence with the privious firmware but there were no bias to any triggers.

The number of sample points shift also disappeared by firmware update. The shift became $< 10^{-7}$ from $\sim 1/2$ on the PIENU data. The gate signal was distributed to the modules which make the WEN and REN signals. The distribution of the latched gate signal resolved the problem.

The reset timing margin became 3.2 ns from 1.2 ns by changing the input from the trigger board to the FINESSE card. The reset or gate signal is using the input on FINESSE although it was only for the gate input. The firmware update allows the input can be useful for two signals. By this update, the long-term stability of time offset between all FINESSEs became extreamly better.

GPIO bcame able to deal with the two level trigger for the digital sum trigger of calorimeter. It saved the 2 μs data dropped by the digital sum trigger. The time stamp on FINESSE also installed and tested. It allows the trigger update of VT48 and VF48 to decrease the deadtime.

These modifications and upgrades made the data of PIENU more stable and reliable. In the following two years (2010 - 2011), the COPPER system will take the data with this firmware.

Bibliography

[1] A. Aguilar-Arevalo. High purity pion beam at triumf. *Nuclear Instruments and Methods in Physics Research A*, 609:102–105, 2009.

[2] Anupama Atre. The search for heavy majorana neutrinos. *JHEP*, 05(030), 2009.

[3] Kaoru Yamada et al. Pion decay-mode tagging in a plastic scintillator using copper 500-mhz fadc. *IEEE transactions on nuclear science*, 54(4):1222, 2007.

[4] Youichi Igarashi et al. A common data acquisition system for high intensity beam experiments. *IEEE*, page 1122, 2004.

[5] Mentor Graphics. *ModelSim*. `http://www.model.com/`.

[6] KEK. Kek-vme system. `http://www-online.kek.jp/~daqplatform/`.

[7] W.J. Marciano and A. Sirlin. hoge. *Phys. Rev. Lett.*, 1993.

[8] Akira Muroi. パイ中間子崩壊分岐比測定実験 pienu のための copper 500 mhz flash adc システムの開発. Master's thesis, 大阪大学大学院理学研究科物理学専攻, 2008.

[9] Xilinx. *Xilinx Manual*. `http://www.xilinx.com/`.

[10] Kaoru Yamada. パイ中間子分岐比測定実験における崩壊モード識別. Master's thesis, 大阪大学大学院理学研究科物理学専攻, 2007.